

FIG. 1

202720-0005/001

Reader Network / Site

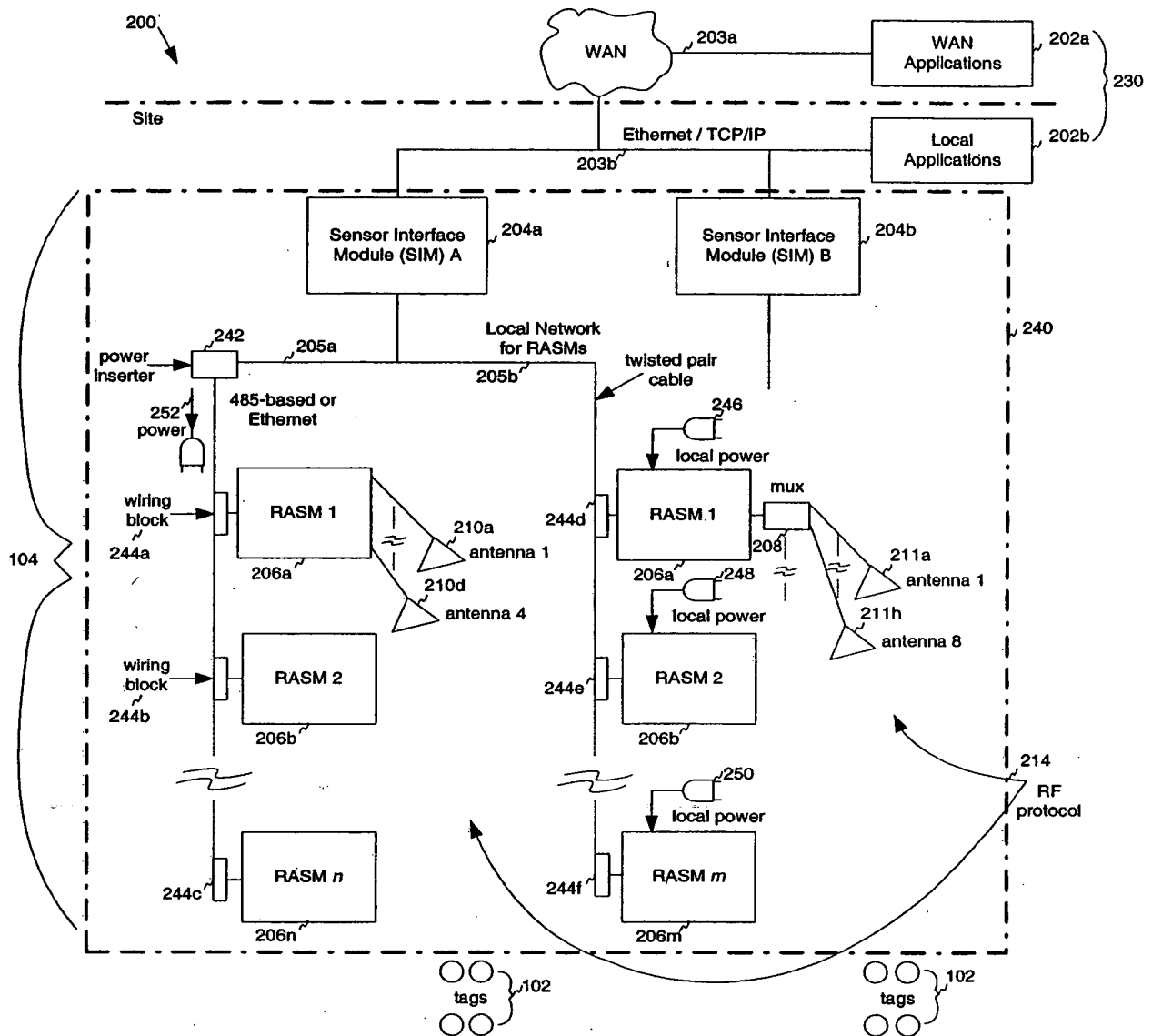


FIG. 2

2007-03-09 00:00:00

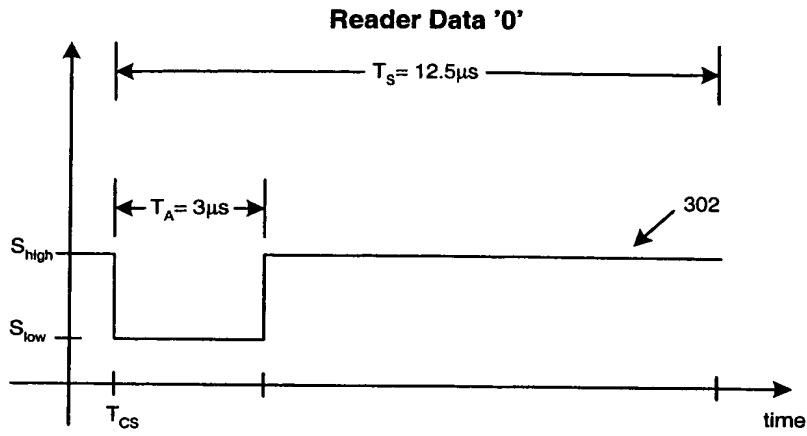


FIG. 3

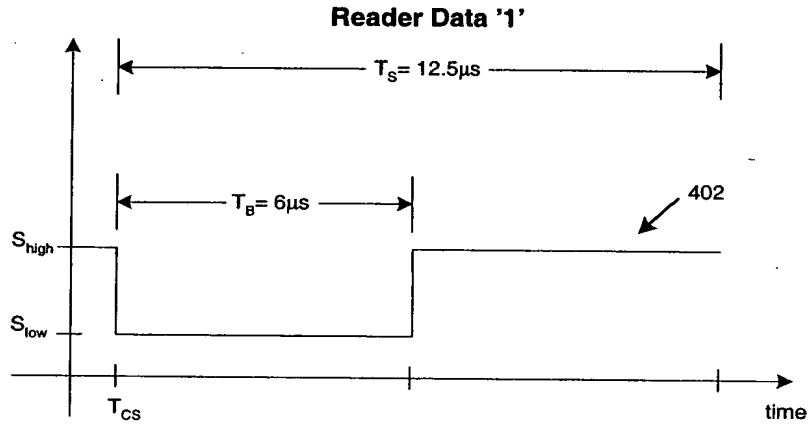


FIG. 4

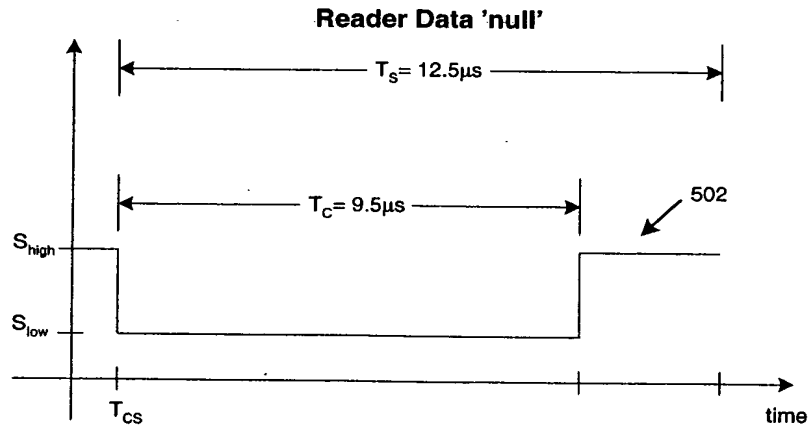


FIG. 5

Reader Bit '0' with Tag Bit '1'

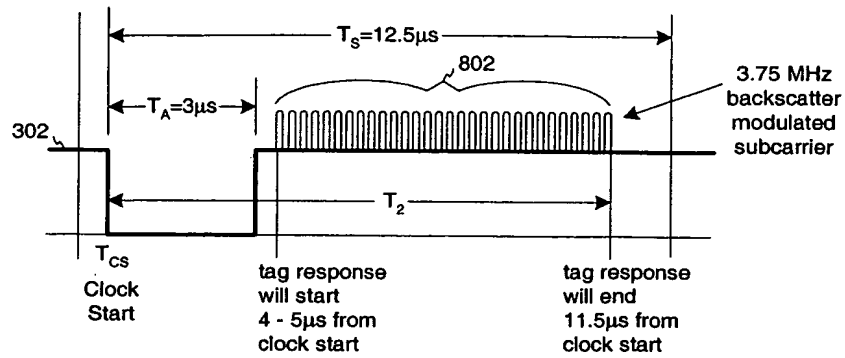


FIG. 8

Reader Bit '1' with Tag Bit '1'

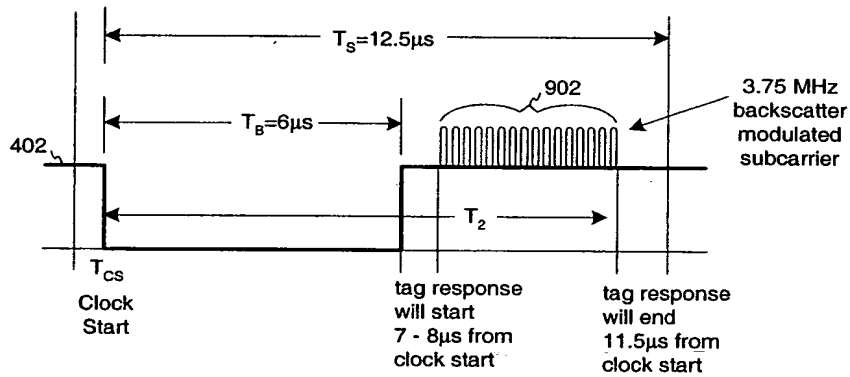


FIG. 9

2001-20b.vsd/6

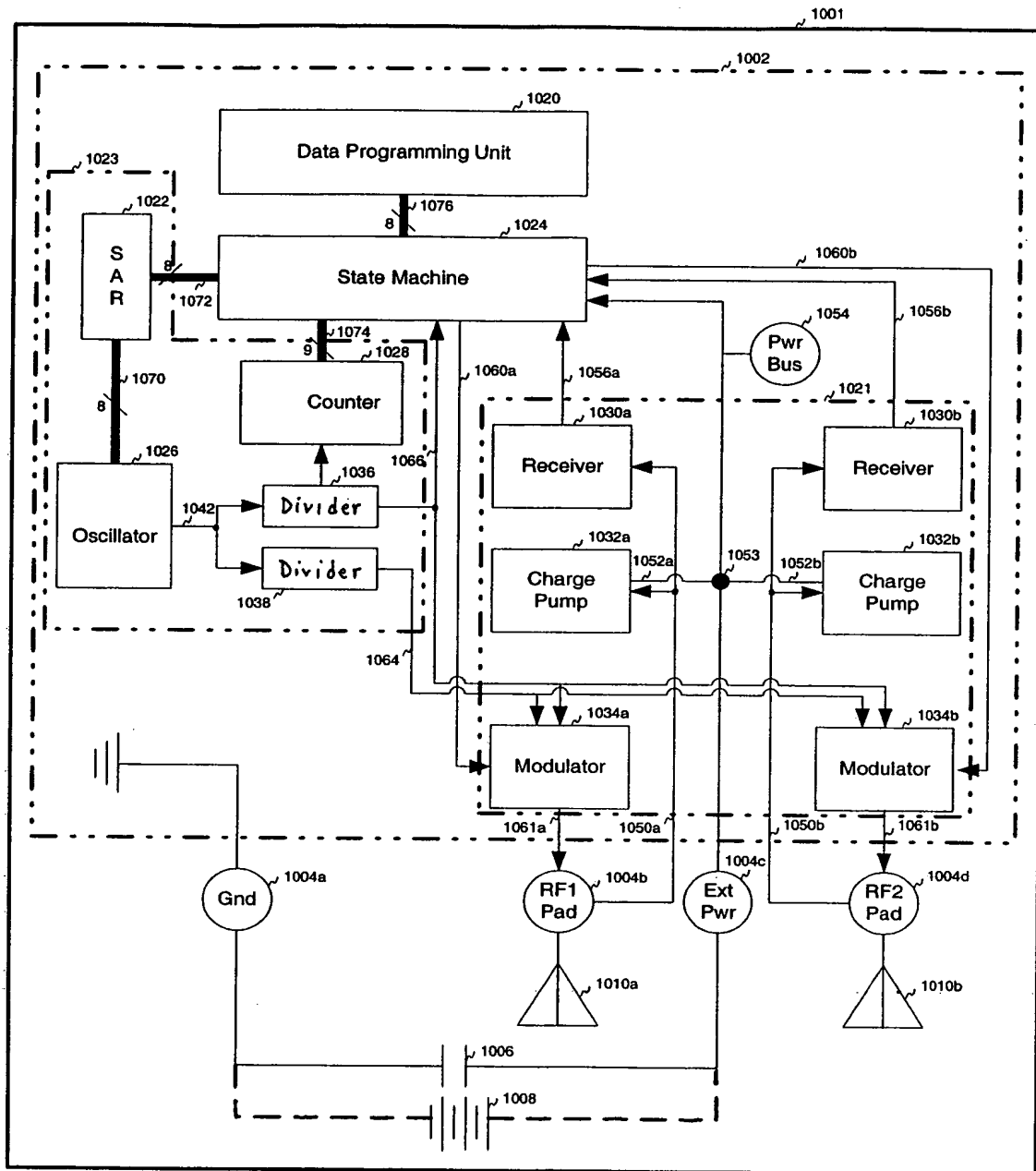


FIG. 10

0201-20b.vsd/7

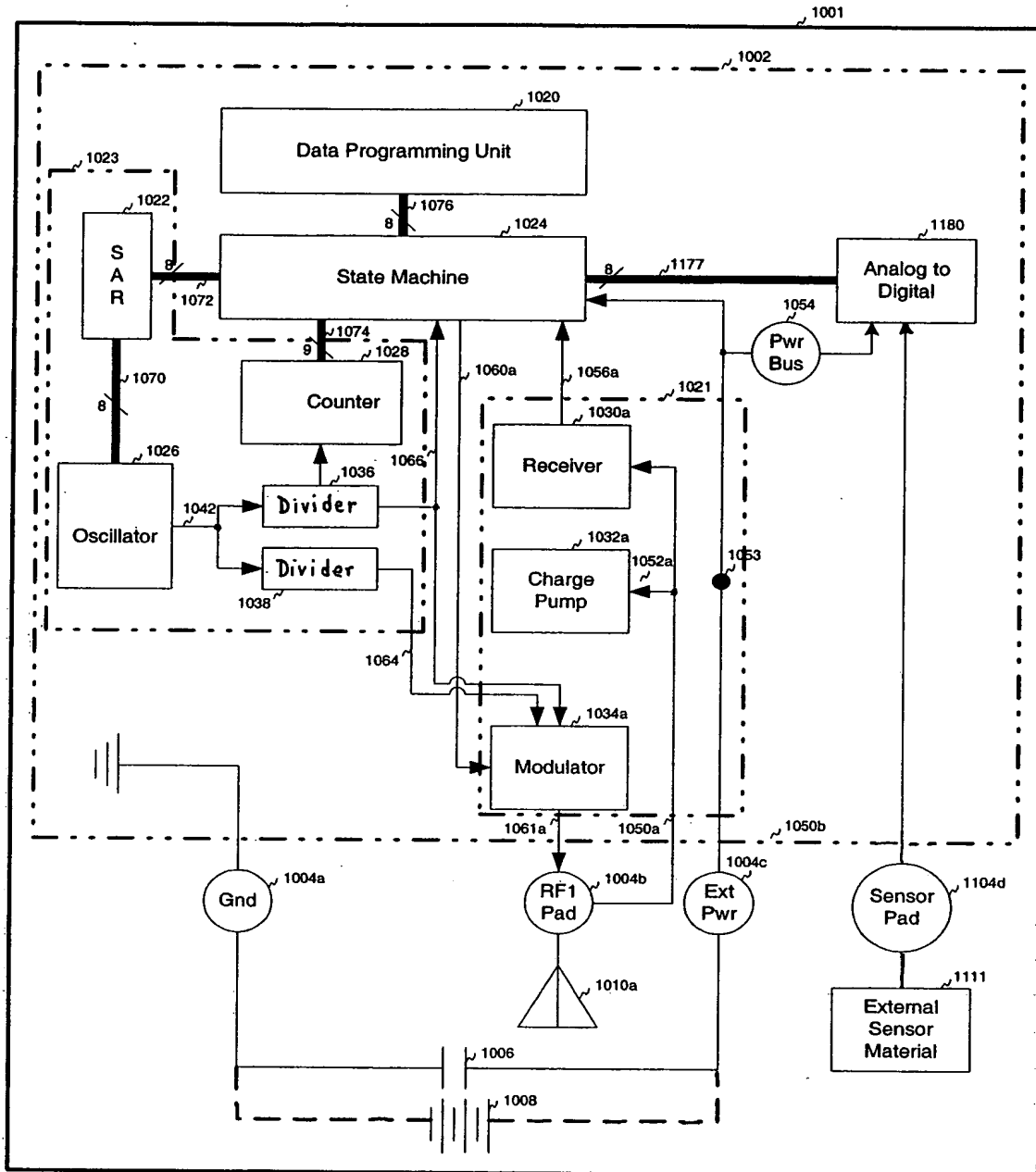


FIG. 11

20073000-001200

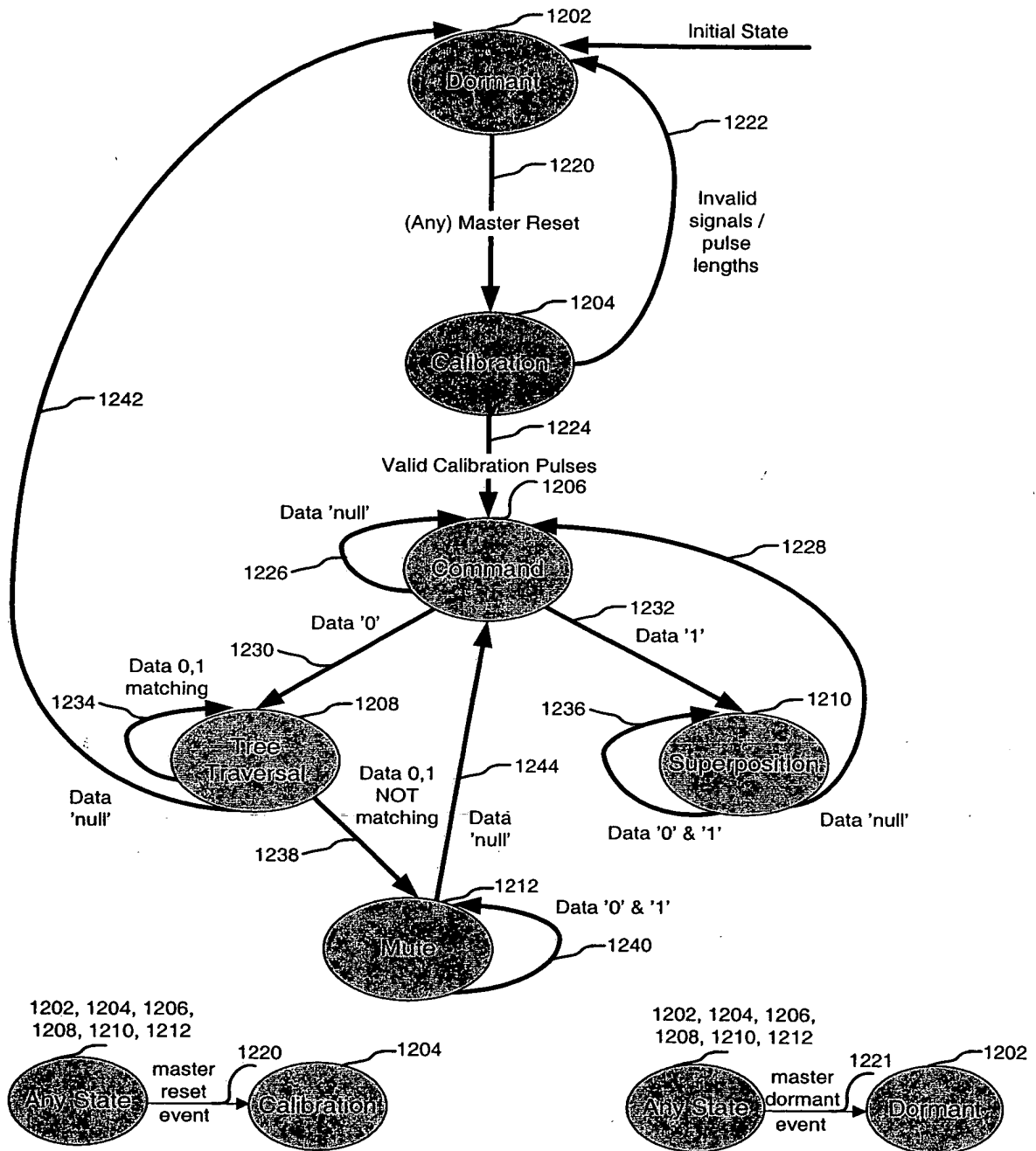


FIG. 12A

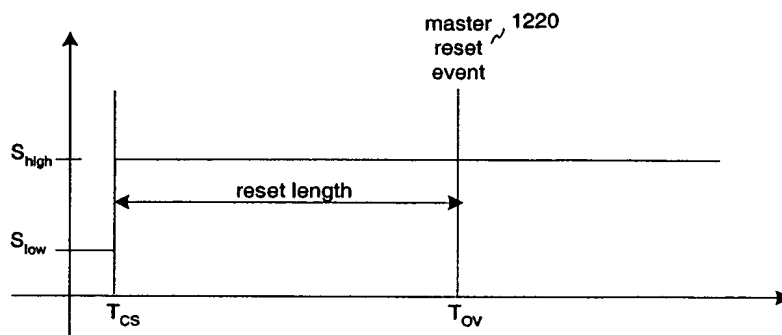


FIG. 12B

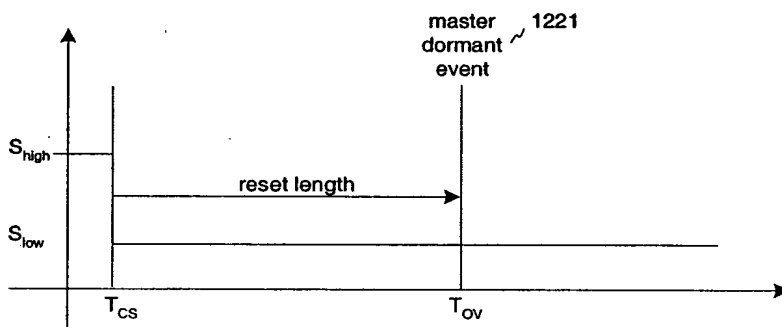


FIG. 12C

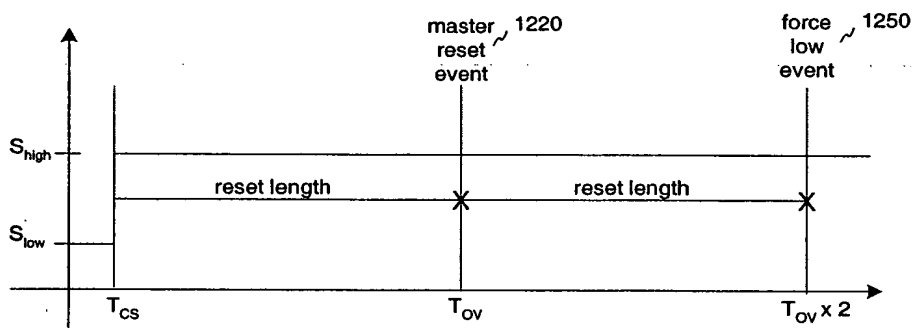


FIG. 12D

THE UNIVERSITY OF CHICAGO



Read Specific Tag, Reader Perspective

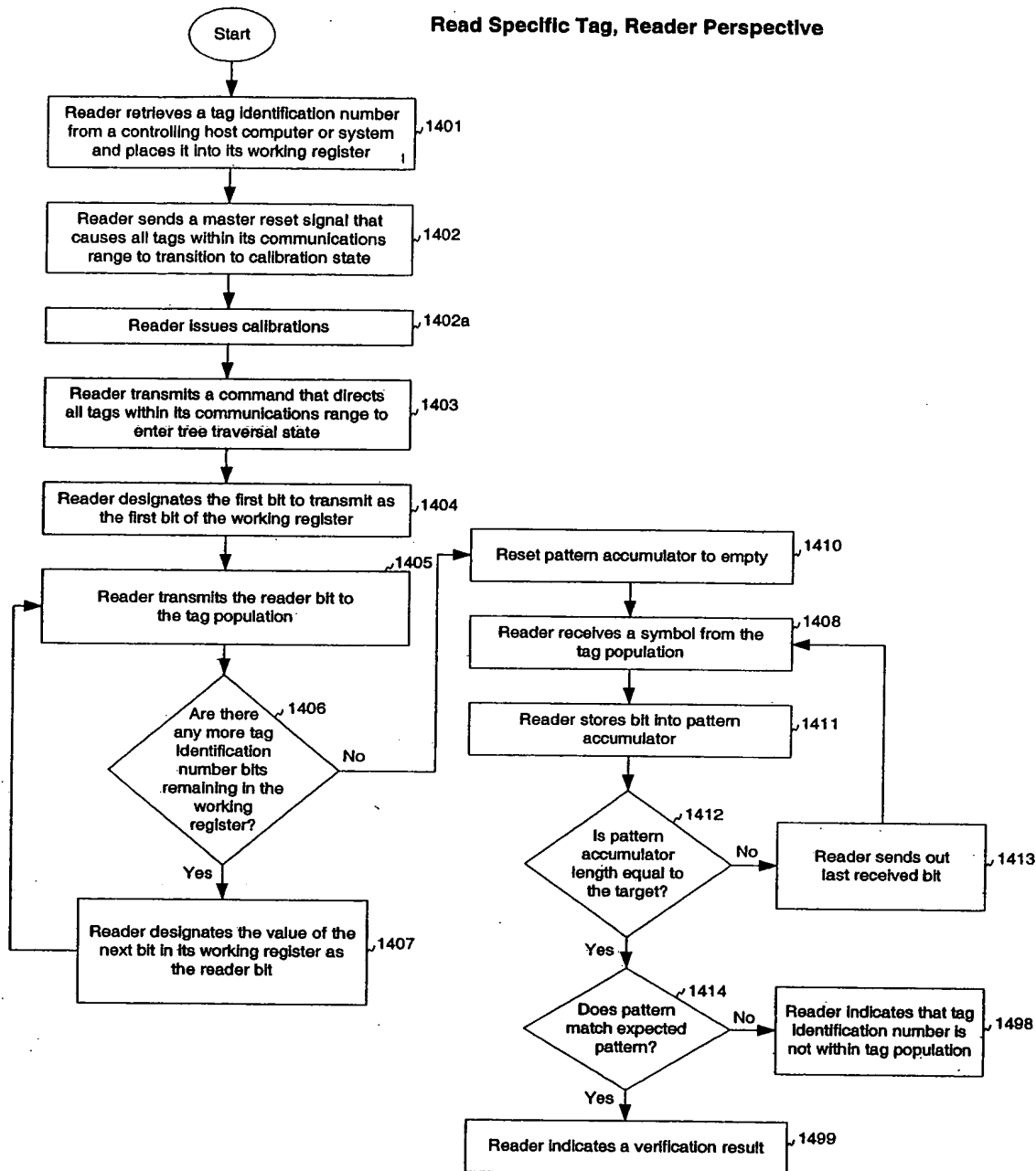


FIG. 14A

2025-03-03 00:00:00

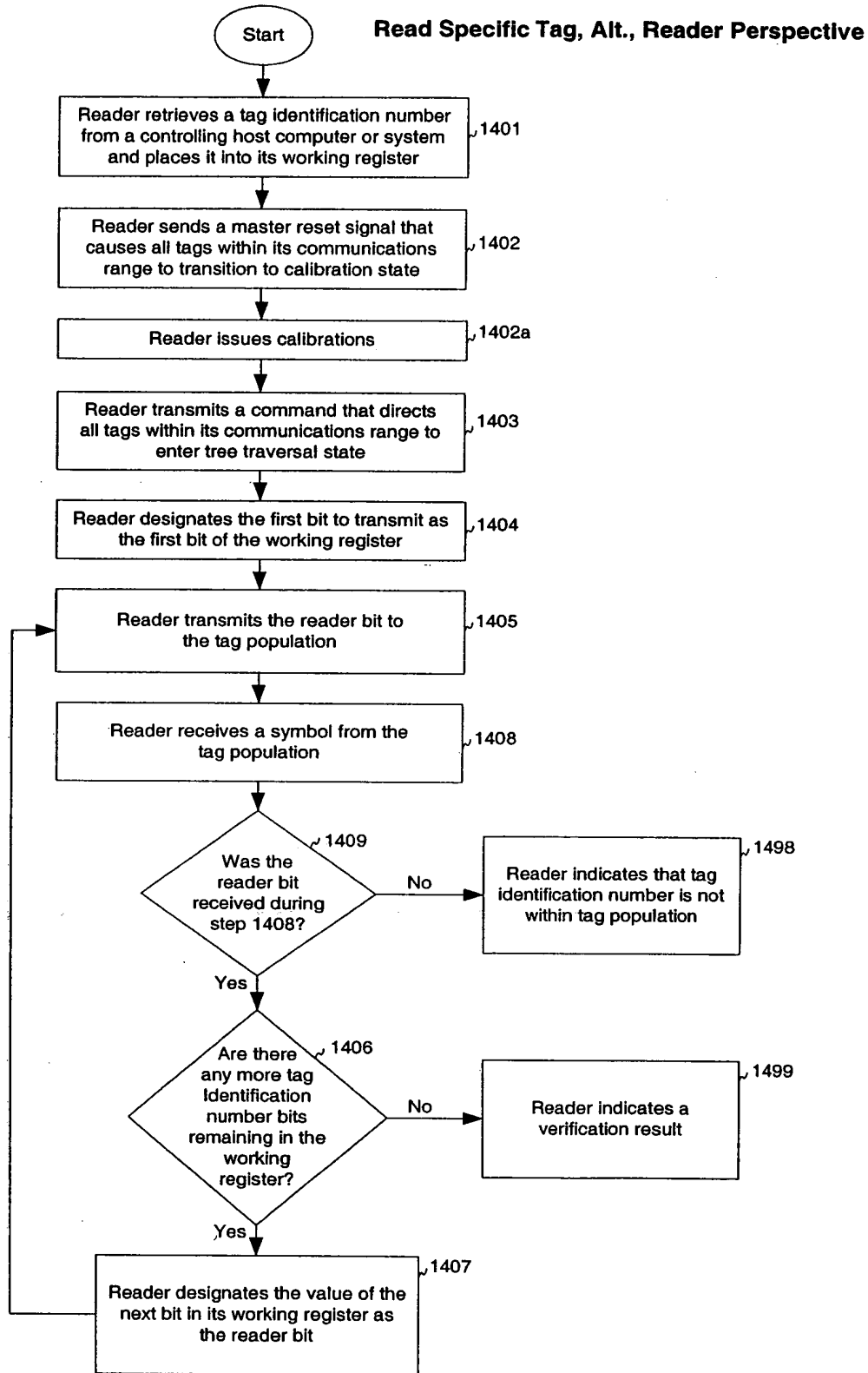


FIG. 14B

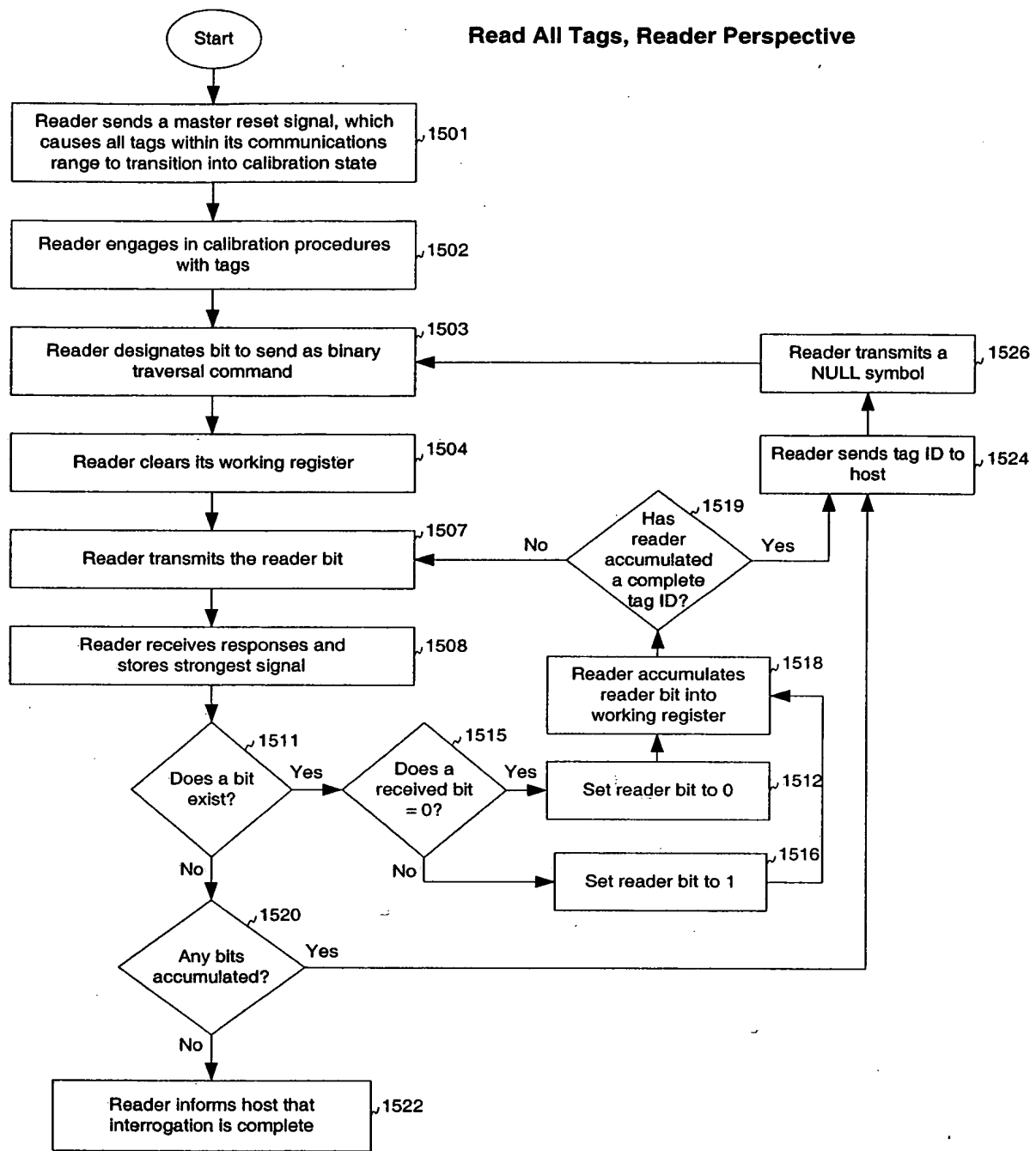


FIG. 15A :

2007-20-0002-001

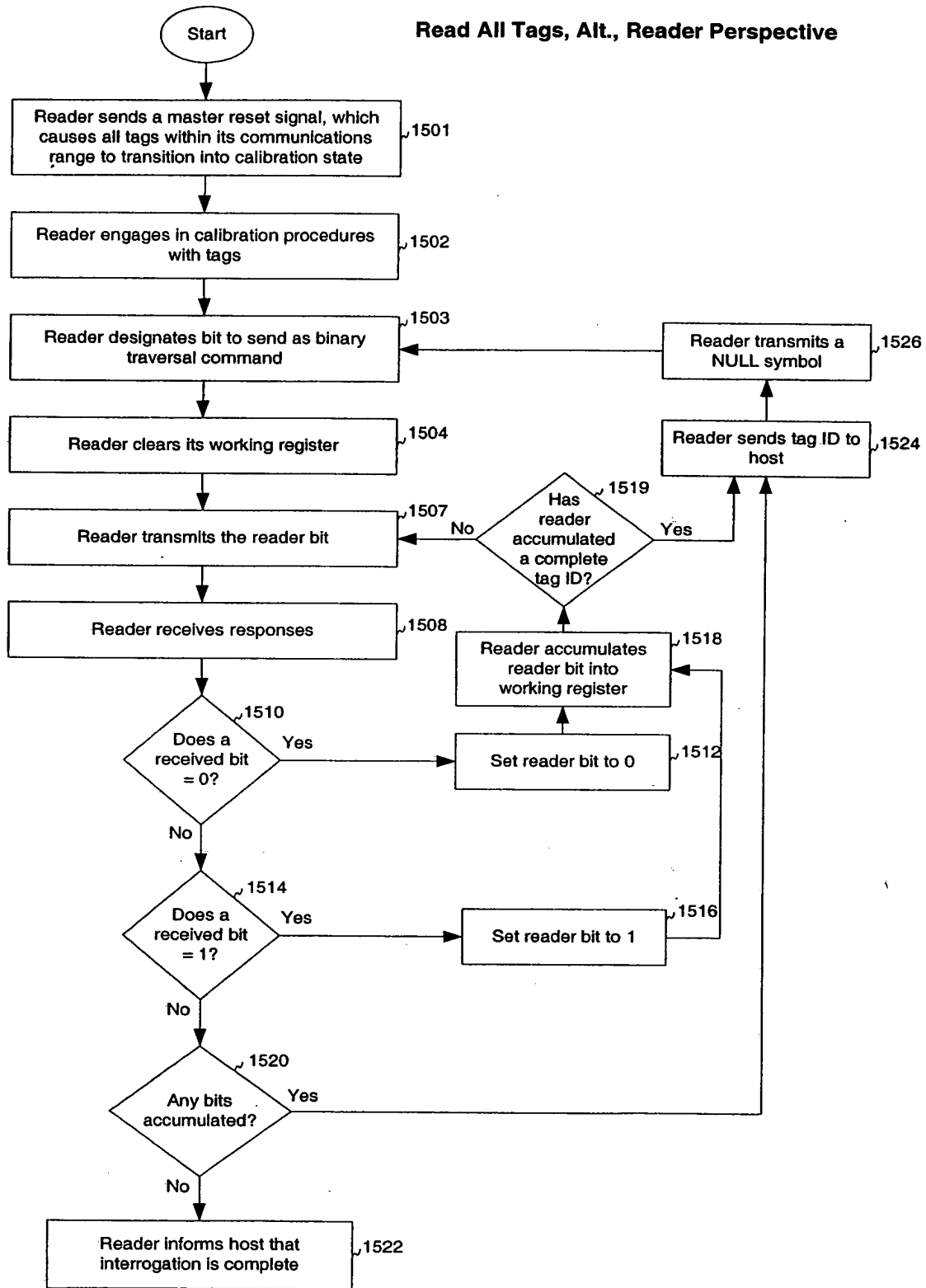


FIG. 15B

Binary Traversal Paths and Tree for a 3-bit Tag Population

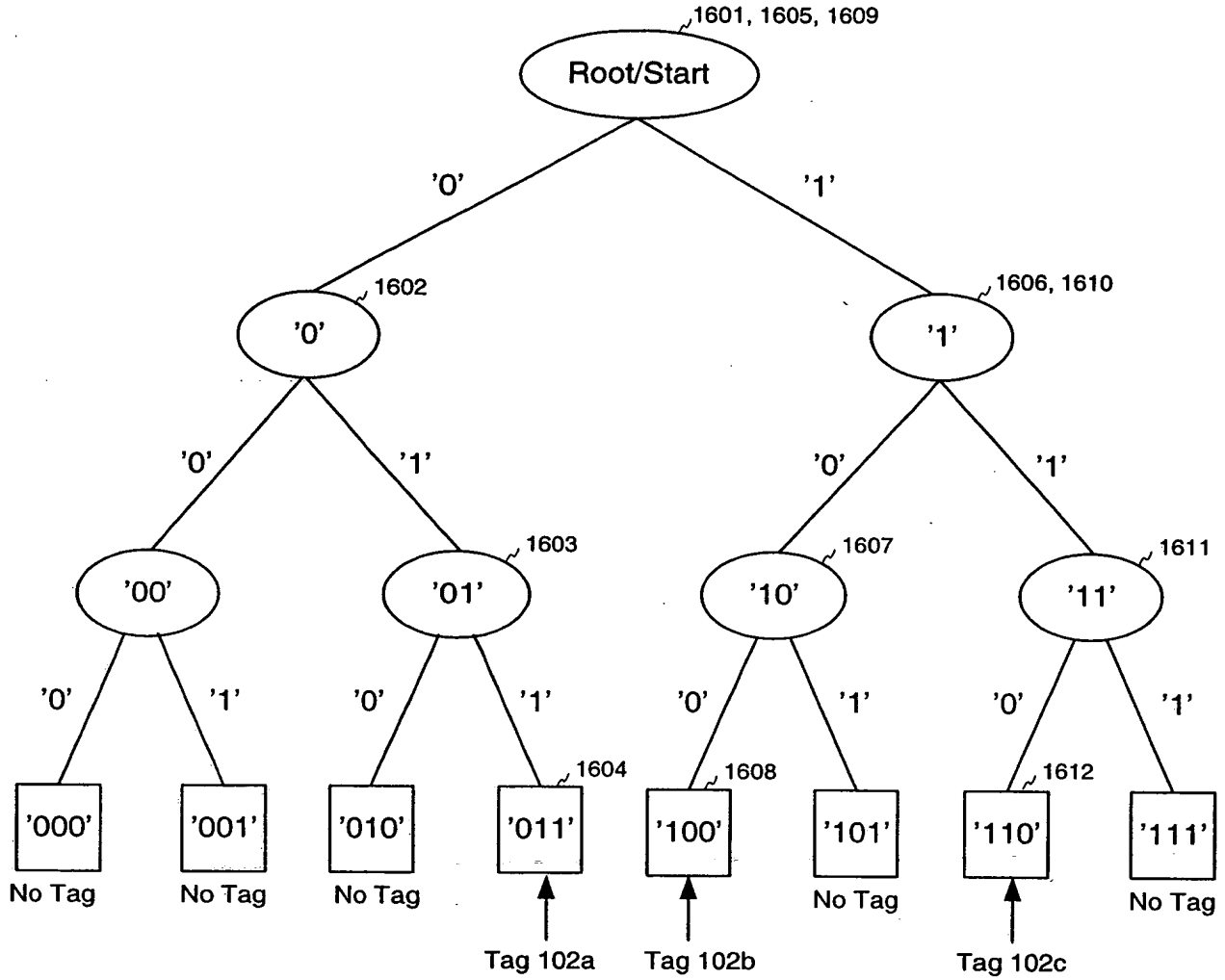


FIG. 16

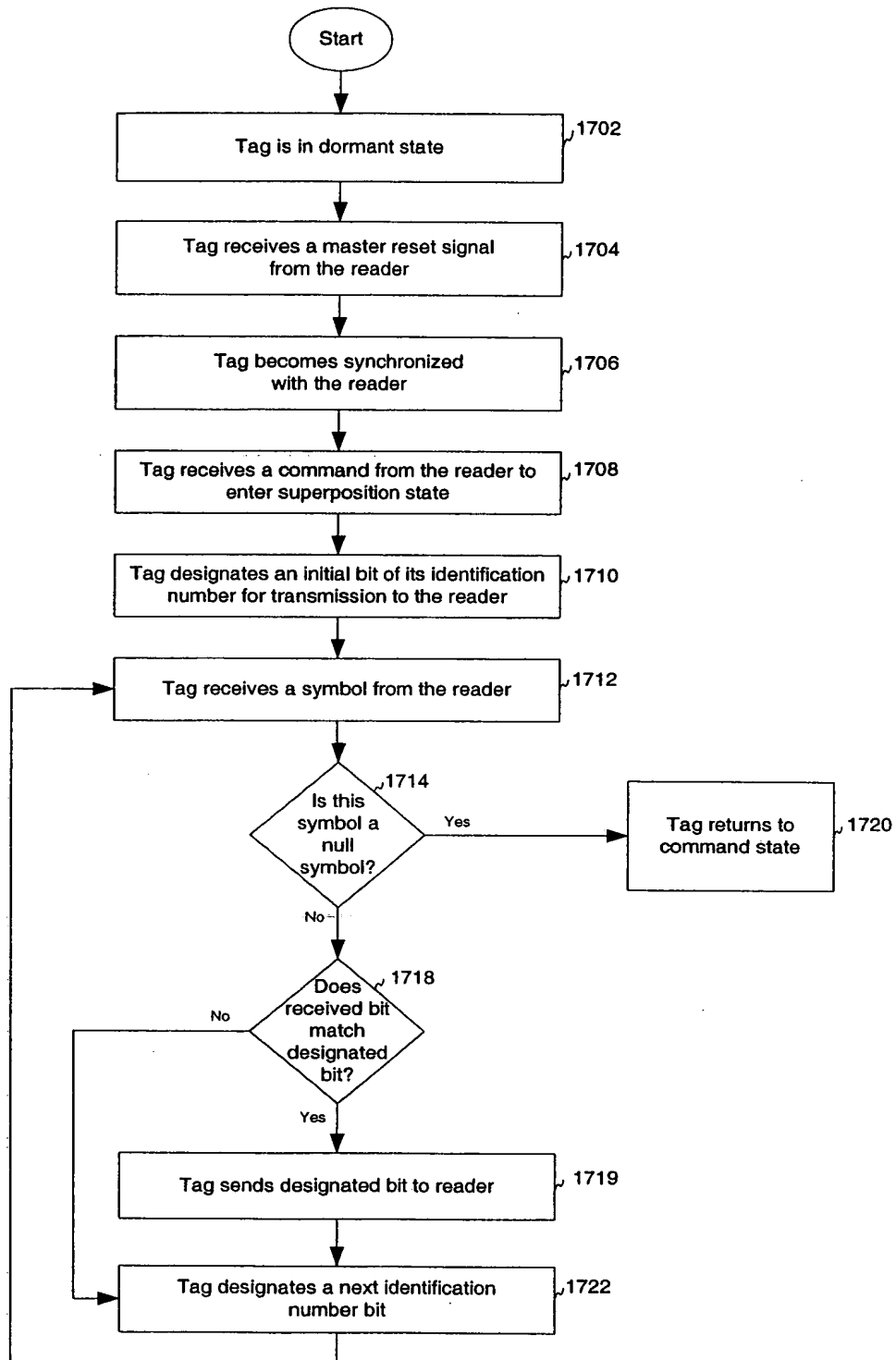


FIG. 17A

2021-20b.vsd/17

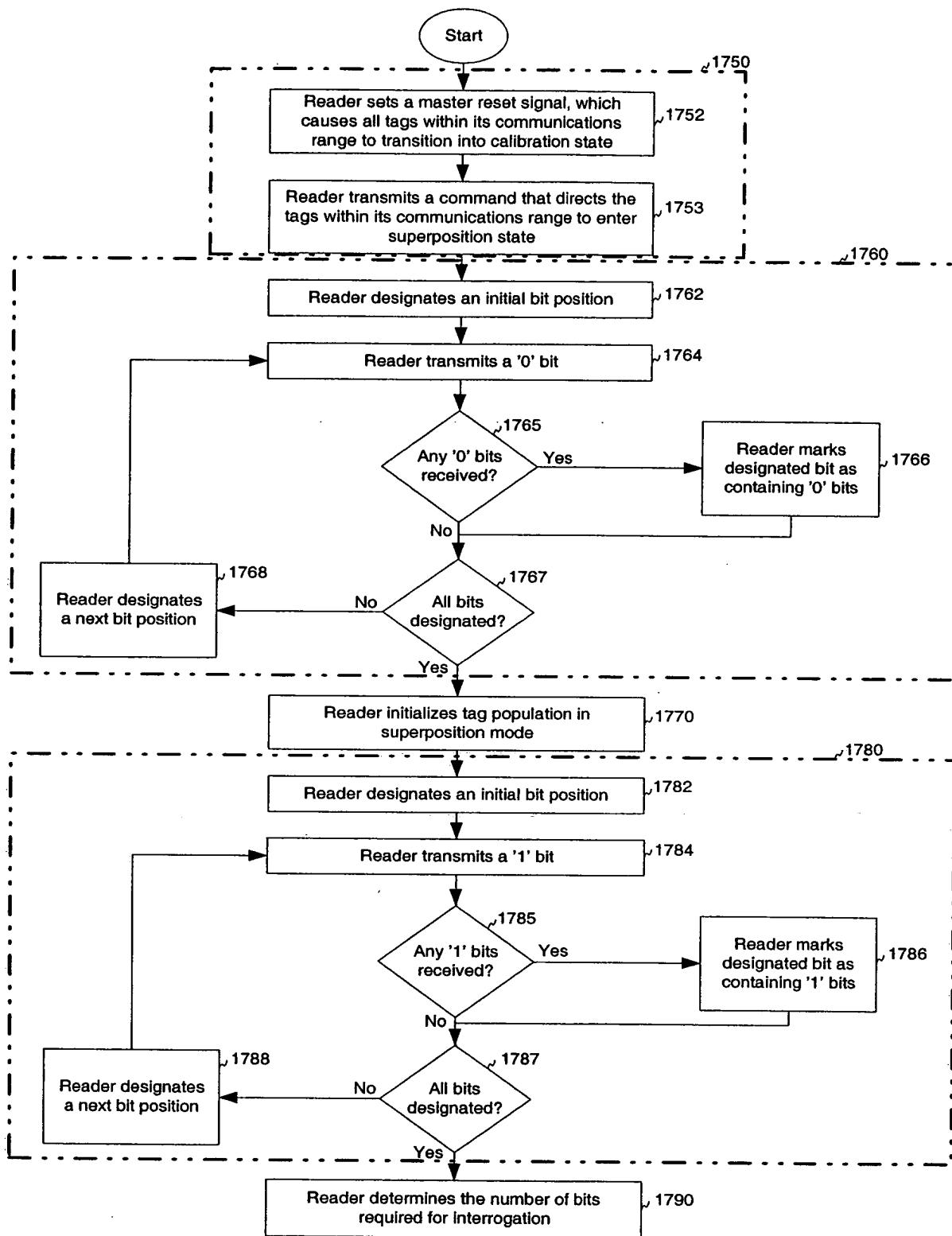


FIG. 17B

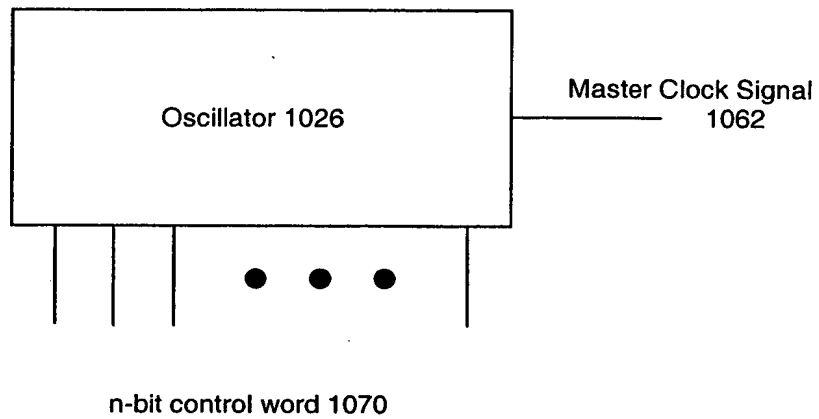


FIG. 18

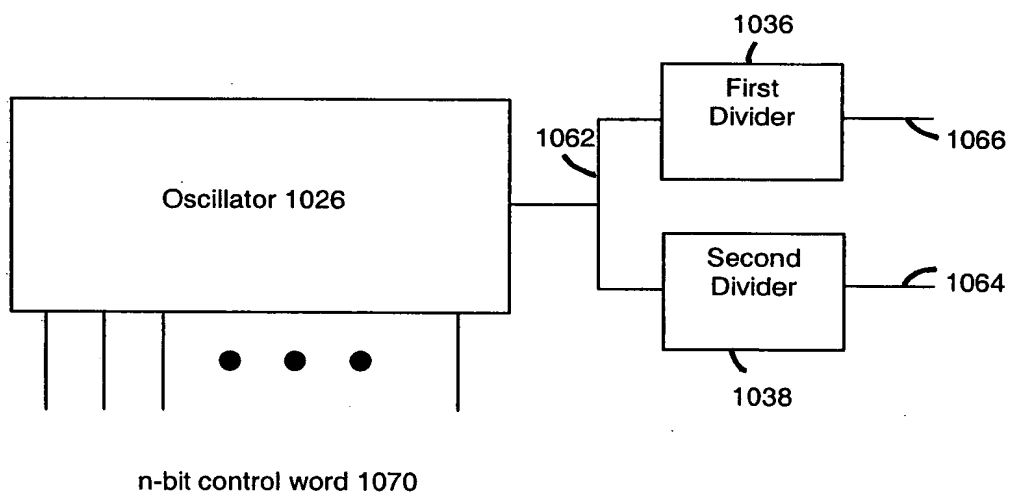


FIG. 19

10073000-004000

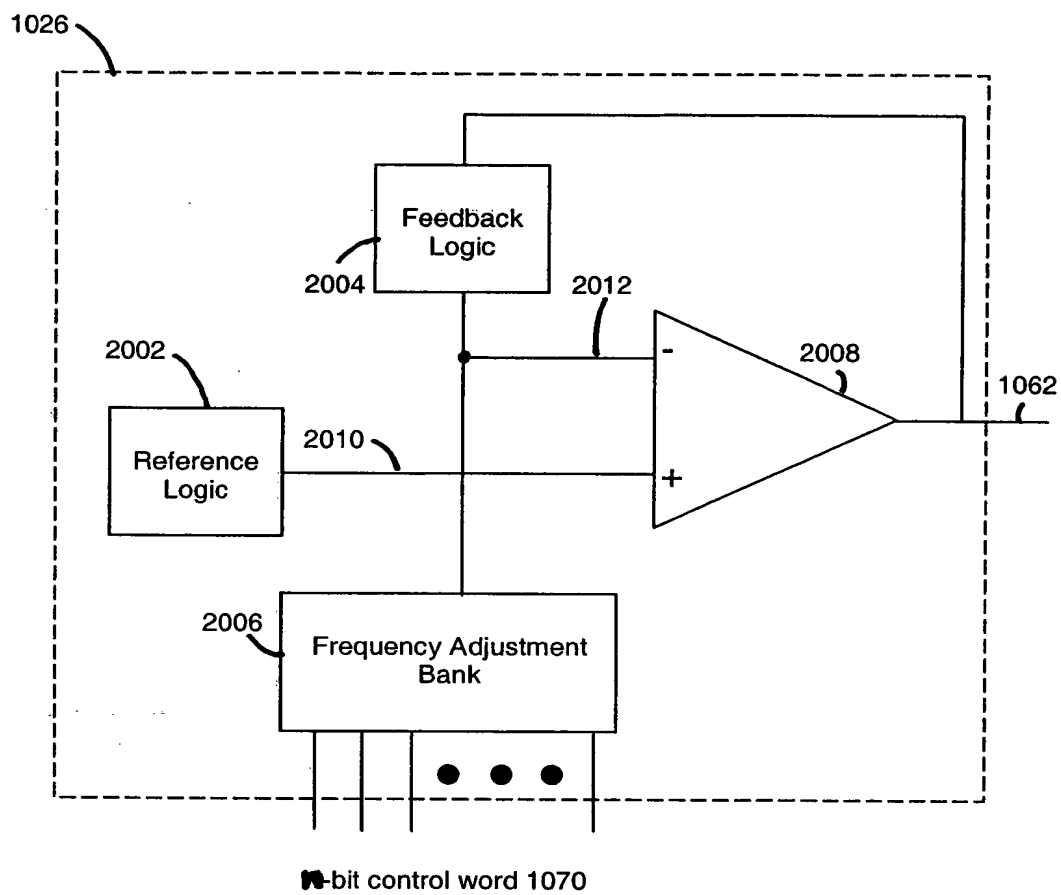


FIG. 20

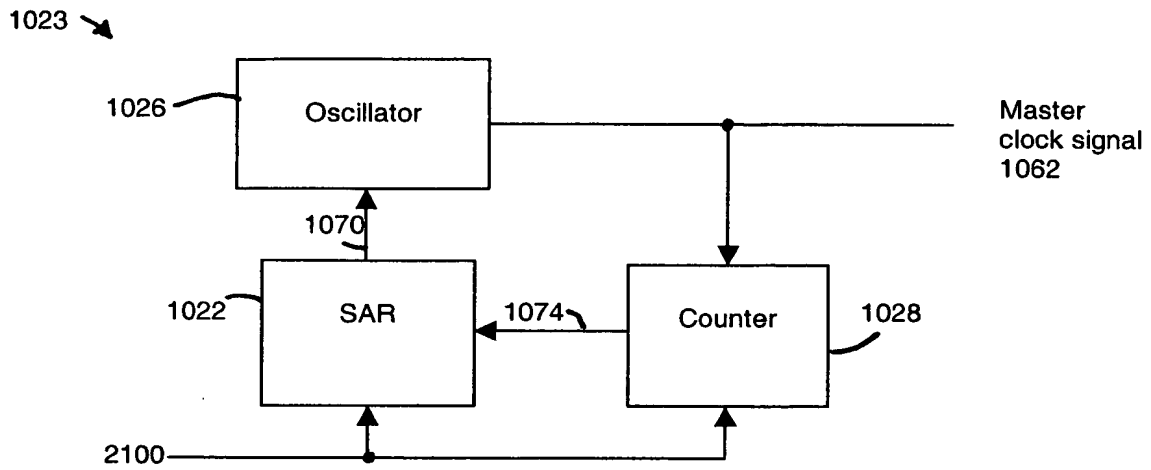


FIG. 21A

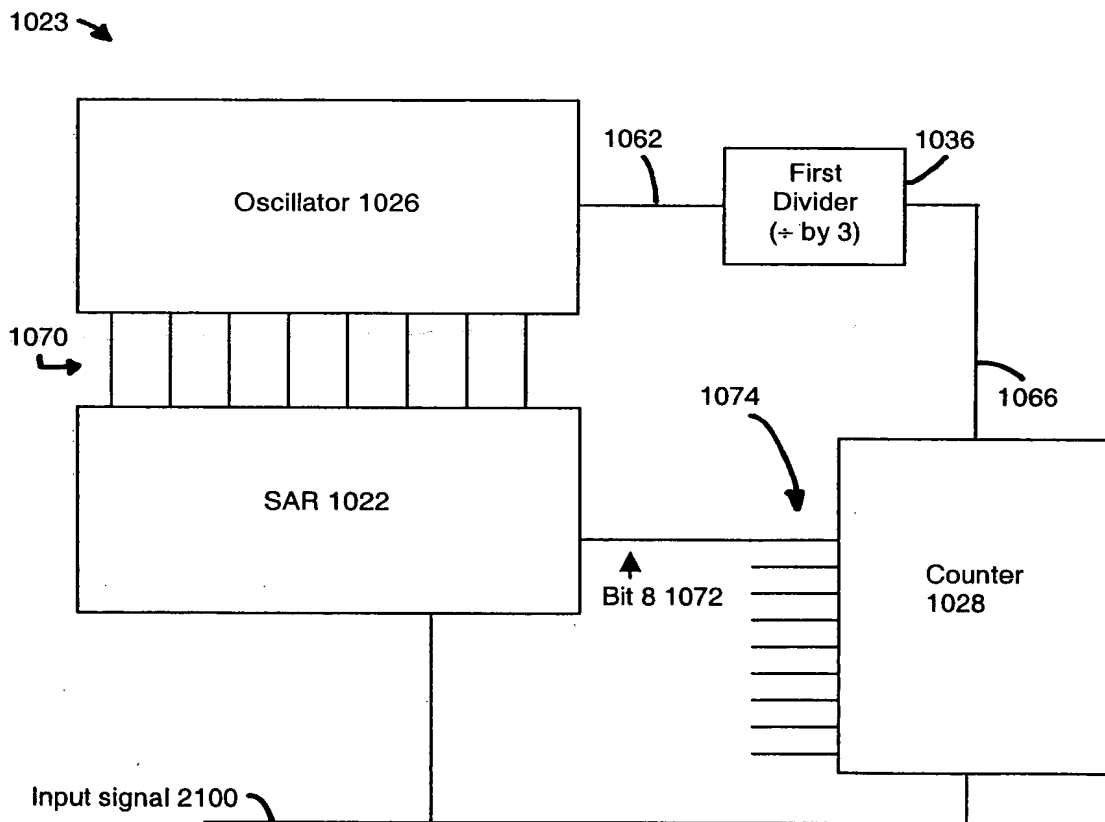


FIG. 21B

Conceptual Implementation of SAR calibration

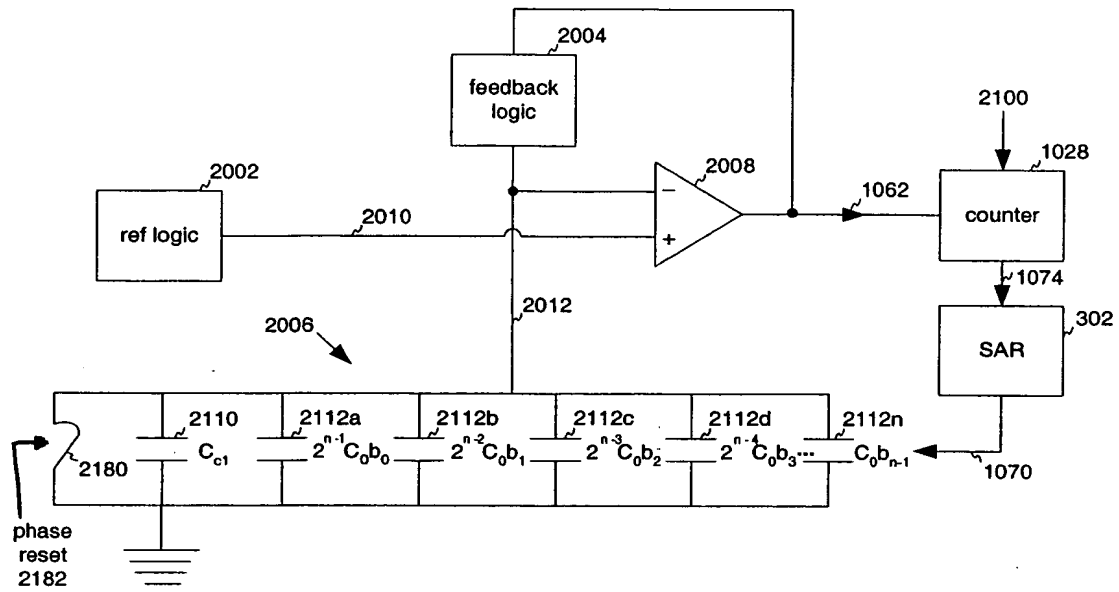


FIG. 21C

Physical implementation of adjustable capacitor bank

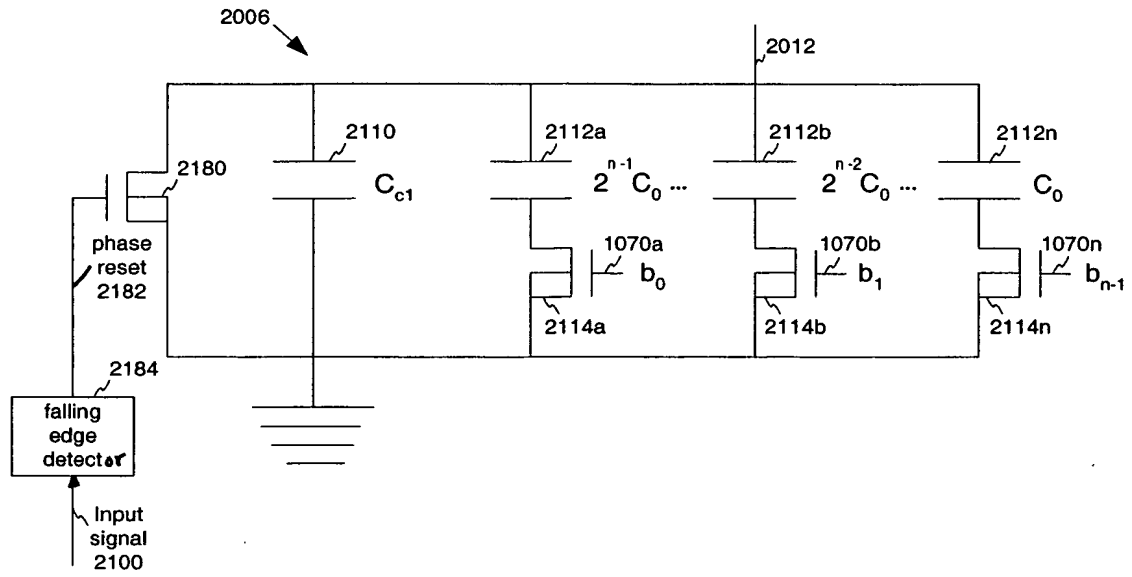
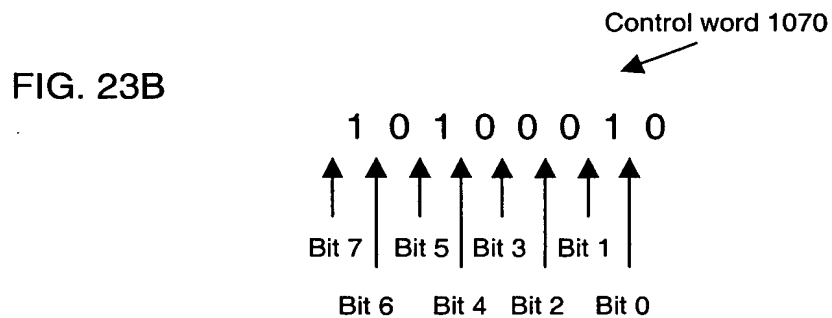
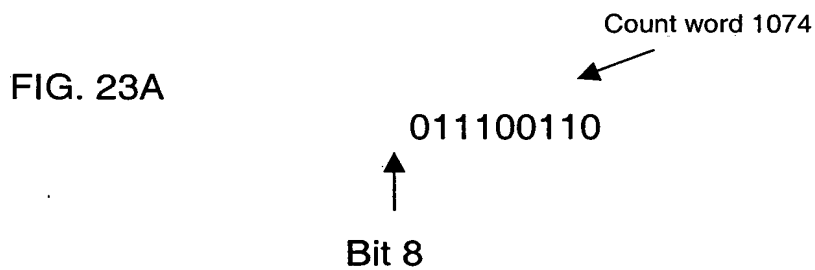
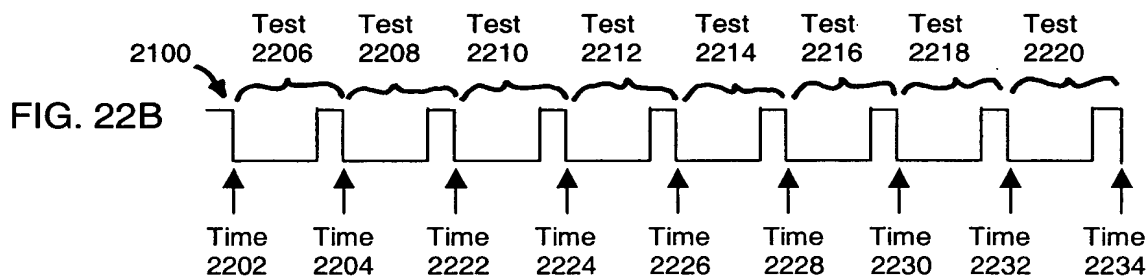
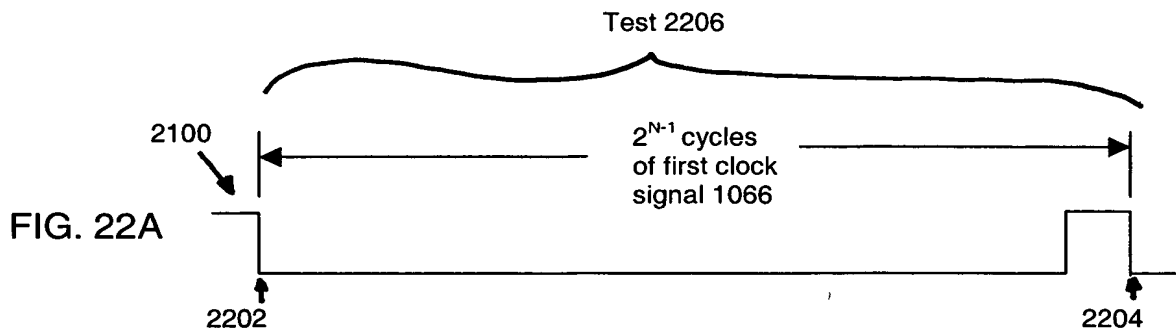


FIG. 21D



2025-03-07 10:20:00

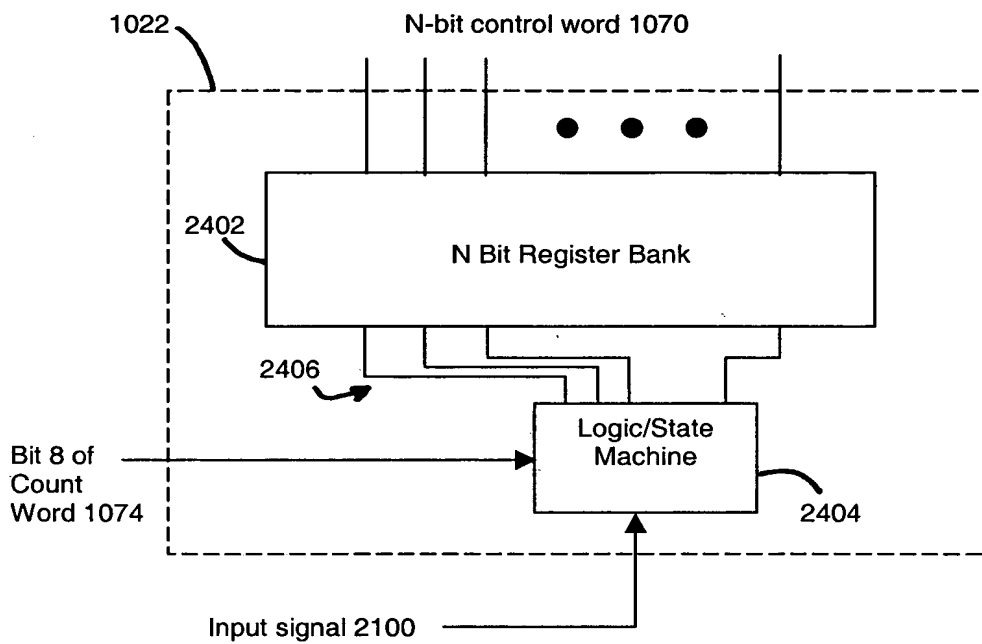


FIG. 24

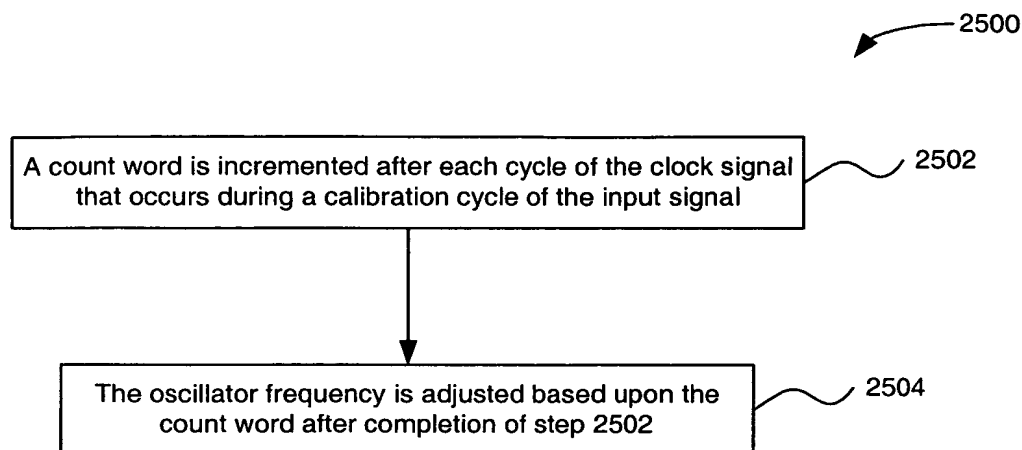


FIG. 25A

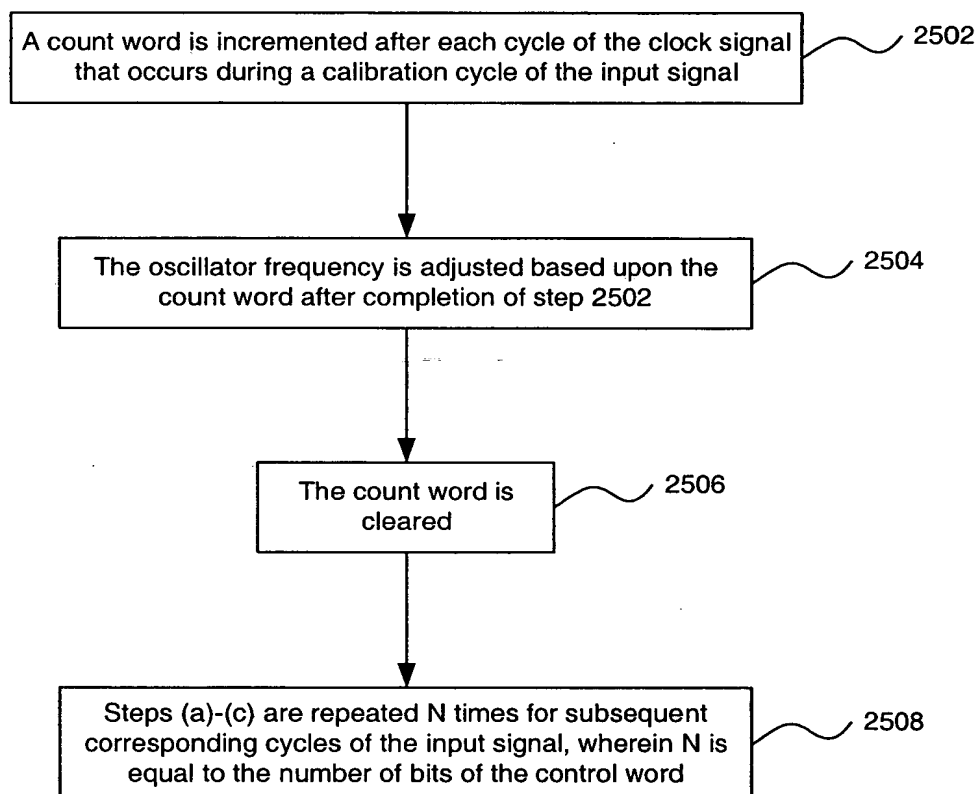


FIG. 25B

```
graph TD; 2502[A count word is incremented after each cycle of the clock signal that occurs during a calibration cycle of the input signal] --> 2504[The oscillator frequency is adjusted based upon the count word after completion of step 2502]; 2504 --> 2510[Each calibration cycle of the input signal followed with a separation cycle on the input signal];
```

A count word is incremented after each cycle of the clock signal that occurs during a calibration cycle of the input signal 2502

The oscillator frequency is adjusted based upon the count word after completion of step 2502 2504

Each calibration cycle of the input signal followed with a separation cycle on the input signal 2510

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2021-02-20 10:00:00

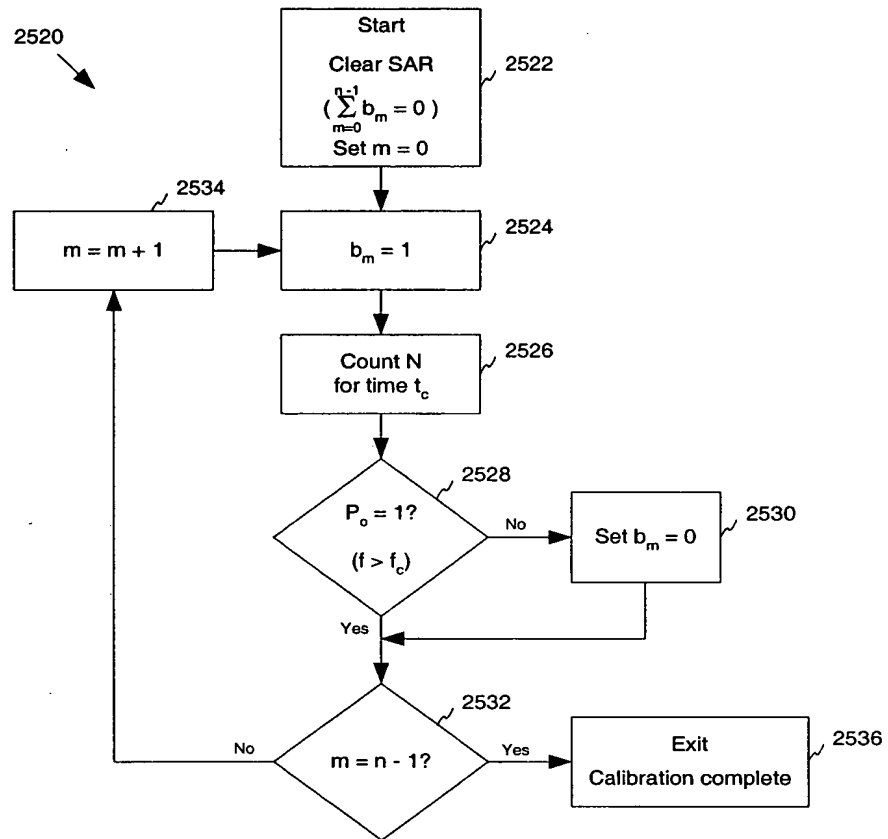


FIG. 25D

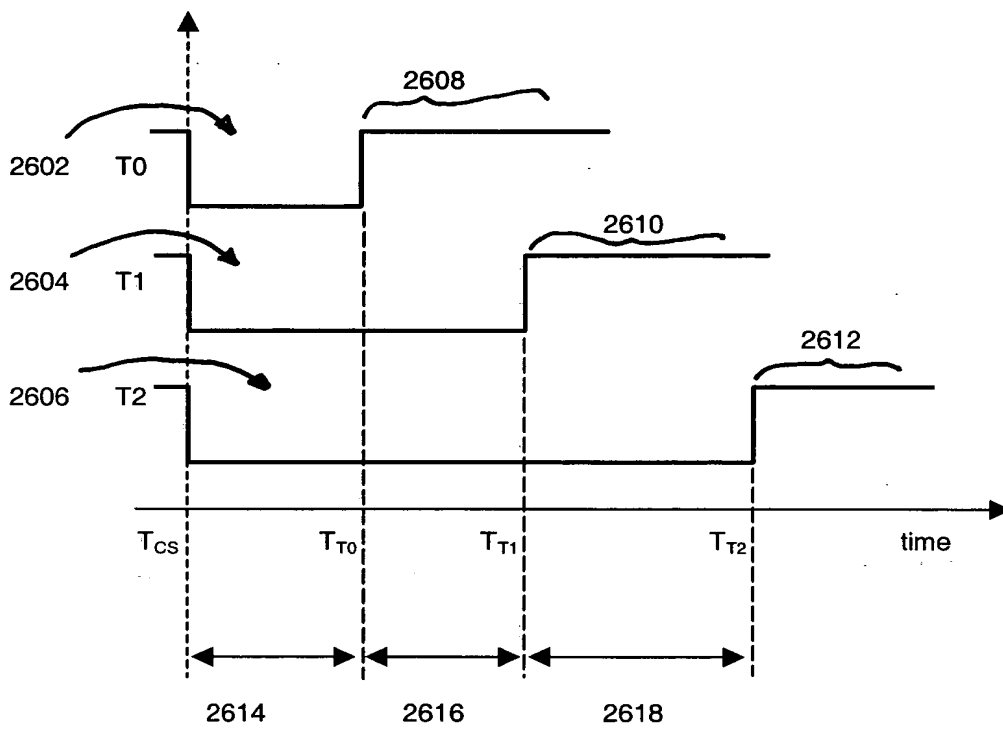


FIG. 26A

2021-20b.vsd/29

Data Symbol Timing Chart

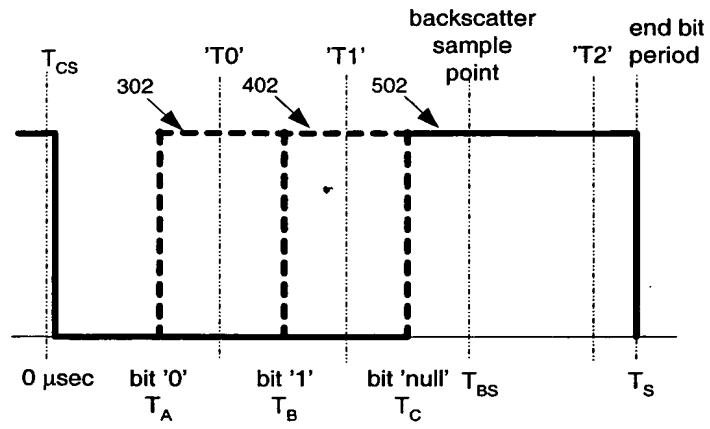


FIG. 26B

2021-20b.vsd/30

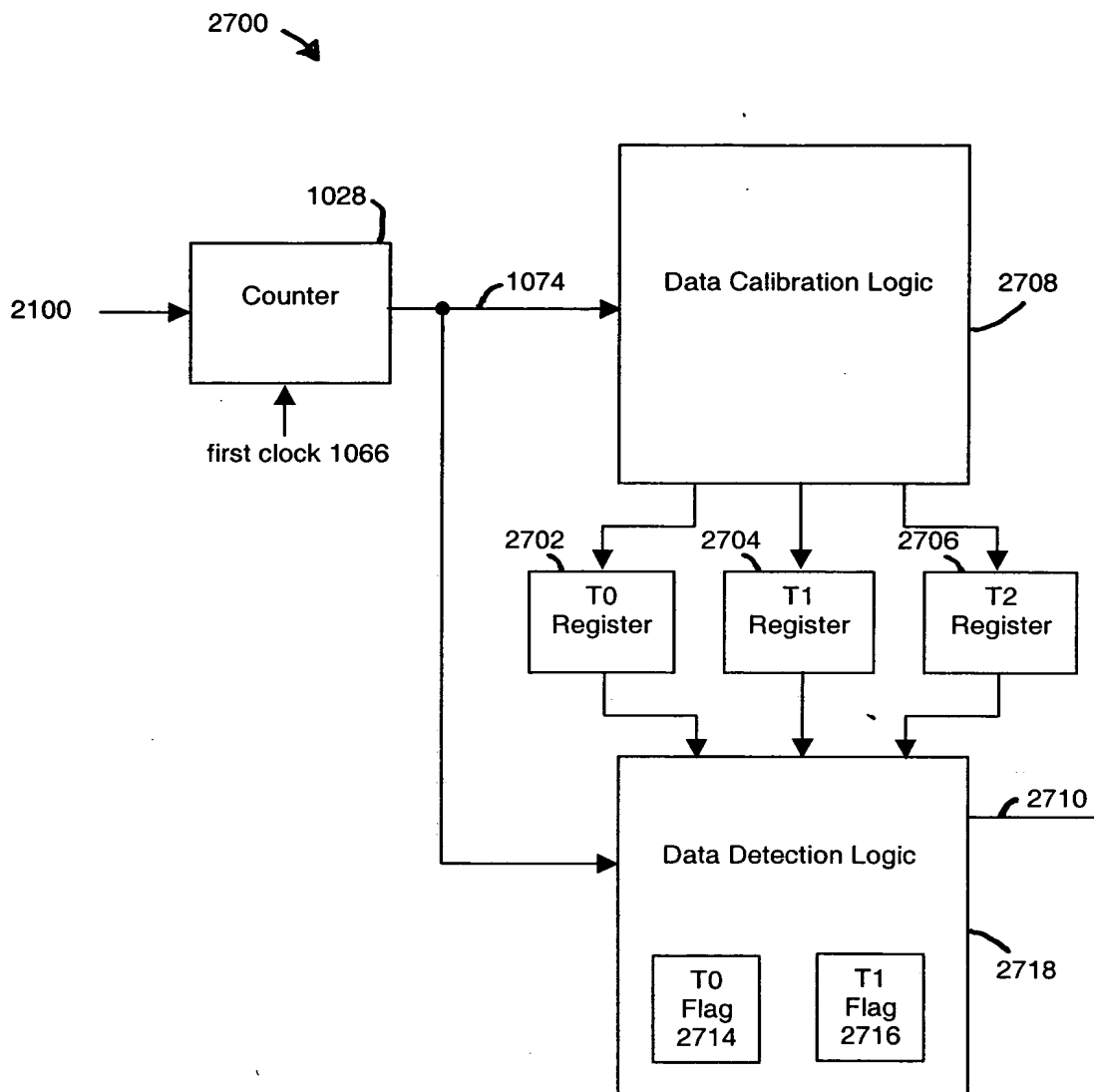


FIG. 27

2800

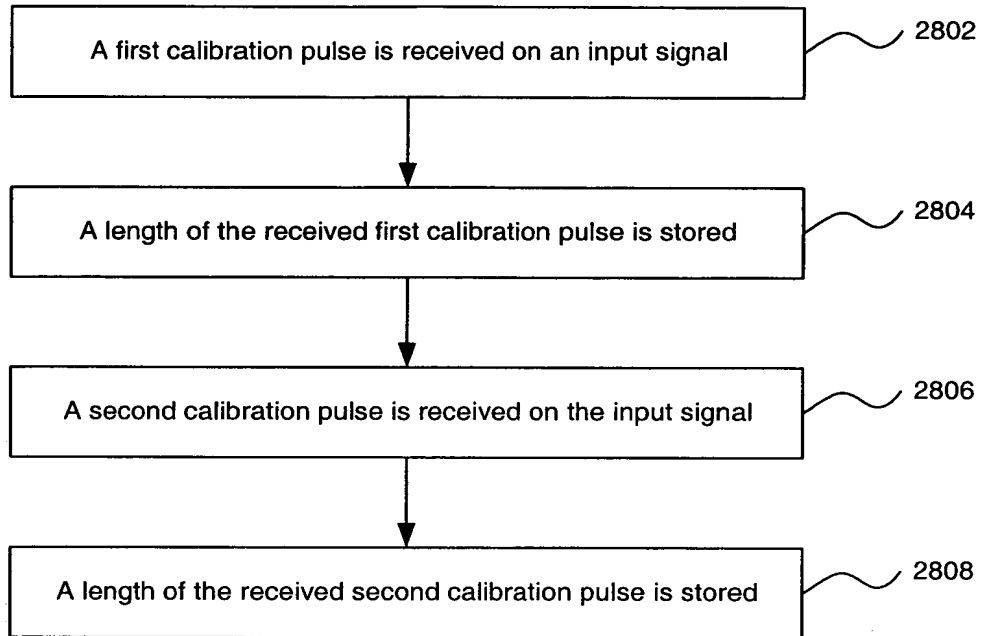


FIG. 28A

2800

From flowchart 2800

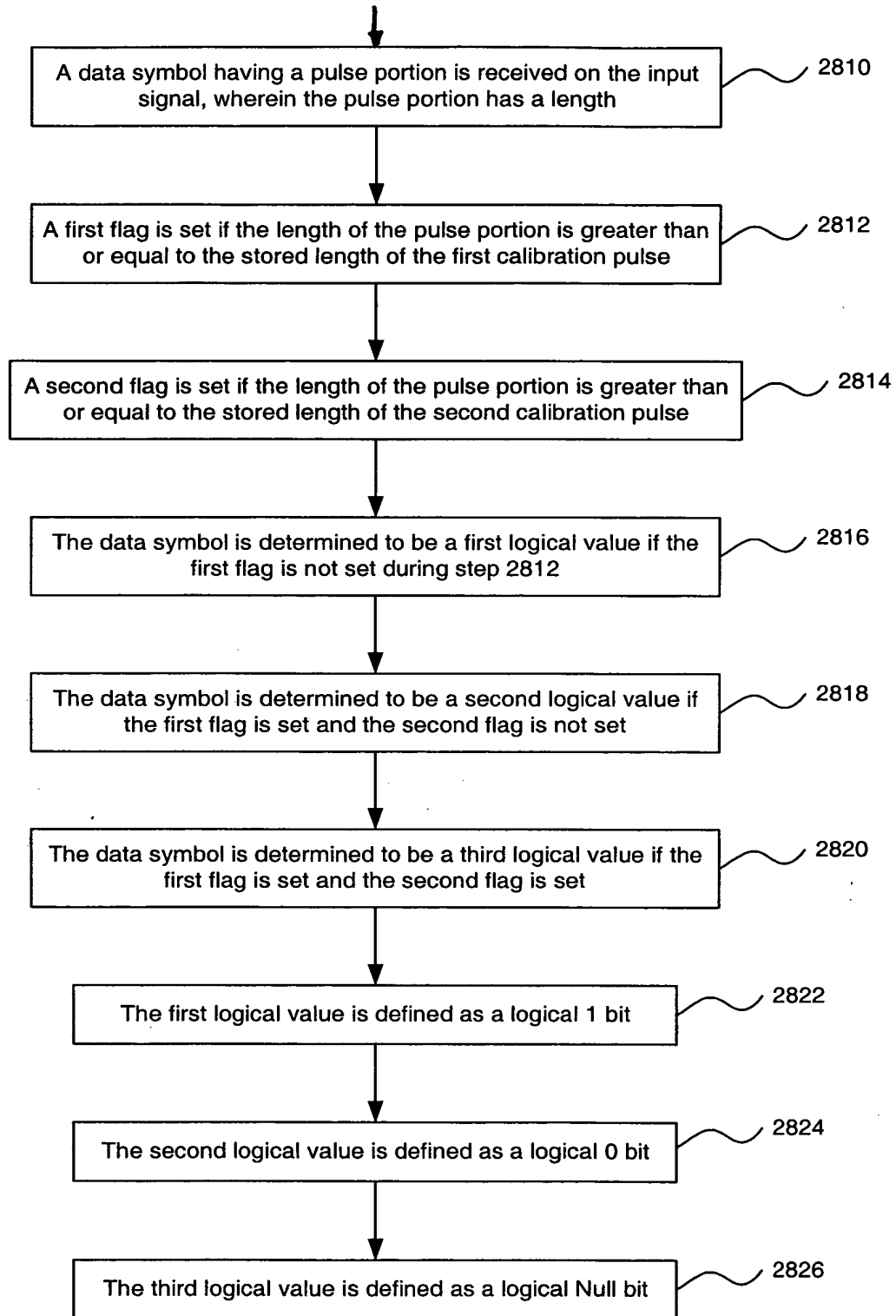


FIG. 28B

10073000-004002

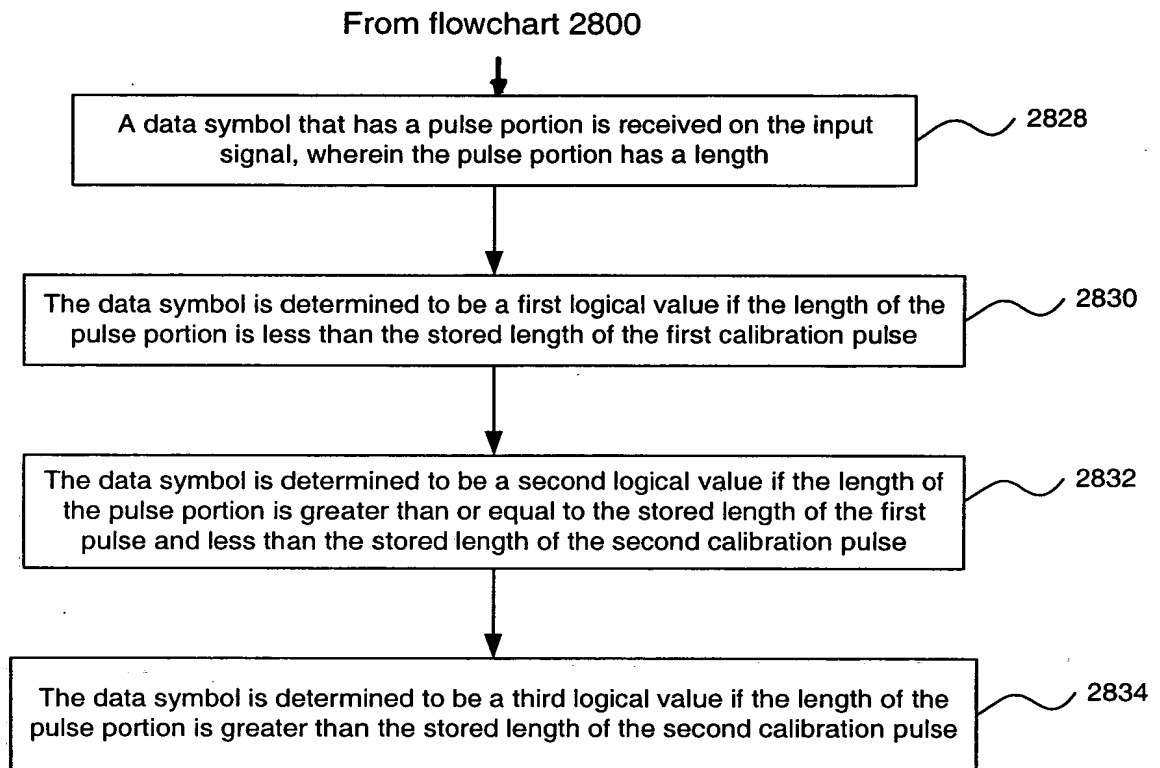


FIG. 28C

2023-08-08 10:00:00

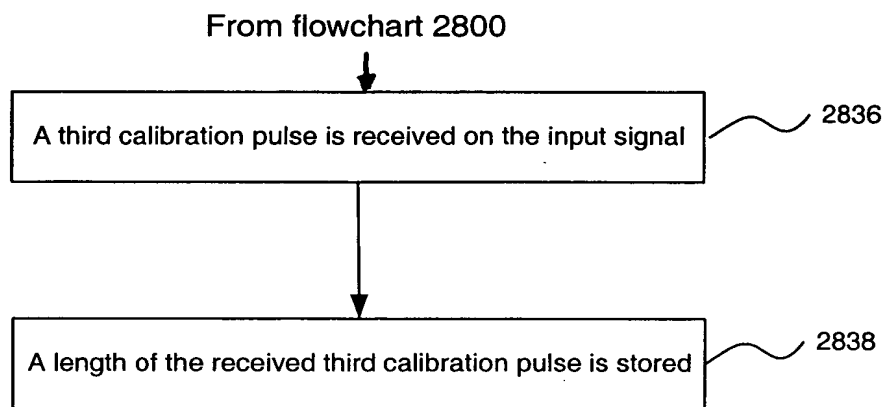


FIG. 28D

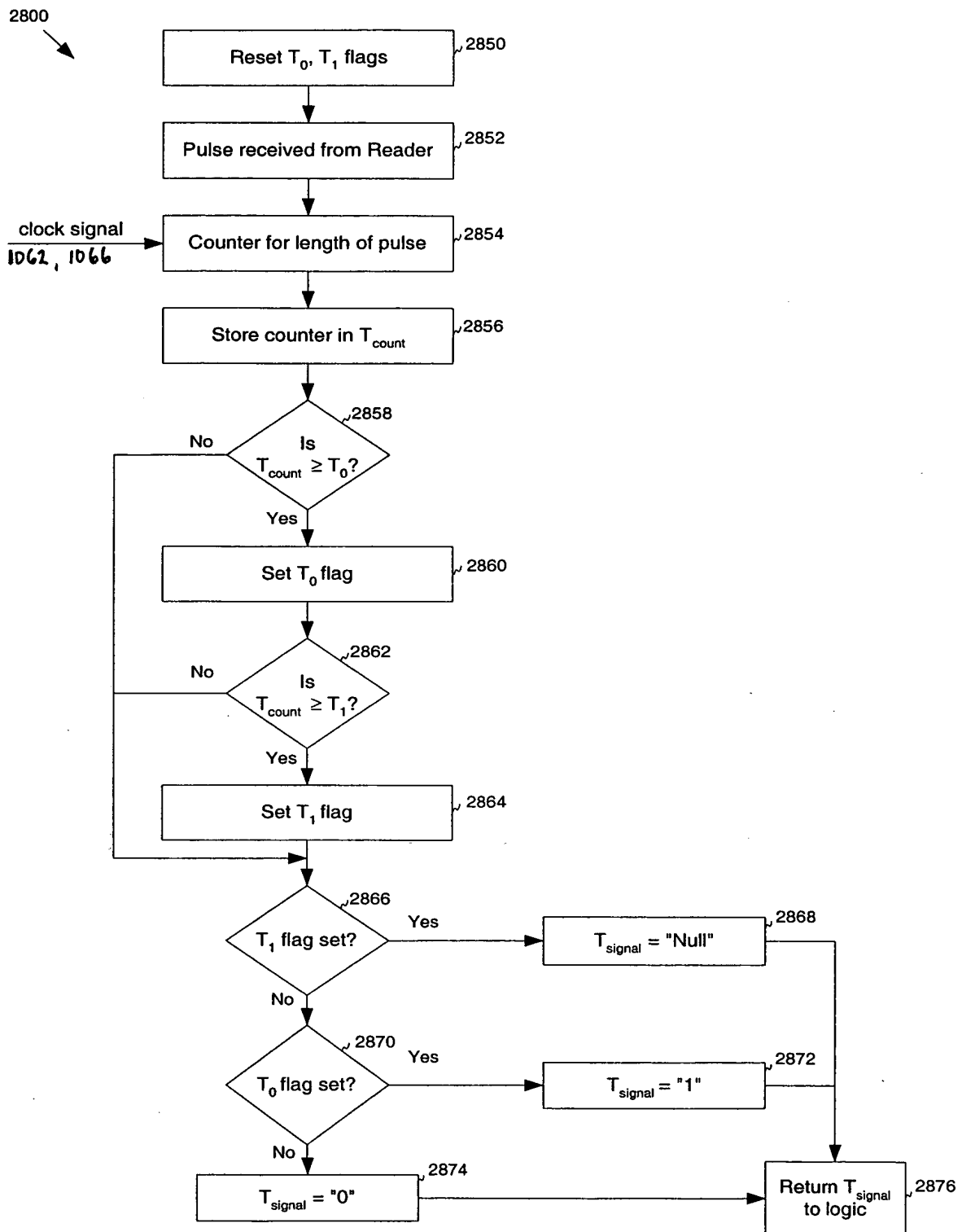


FIG. 28E

2025-03-29 09:00:00

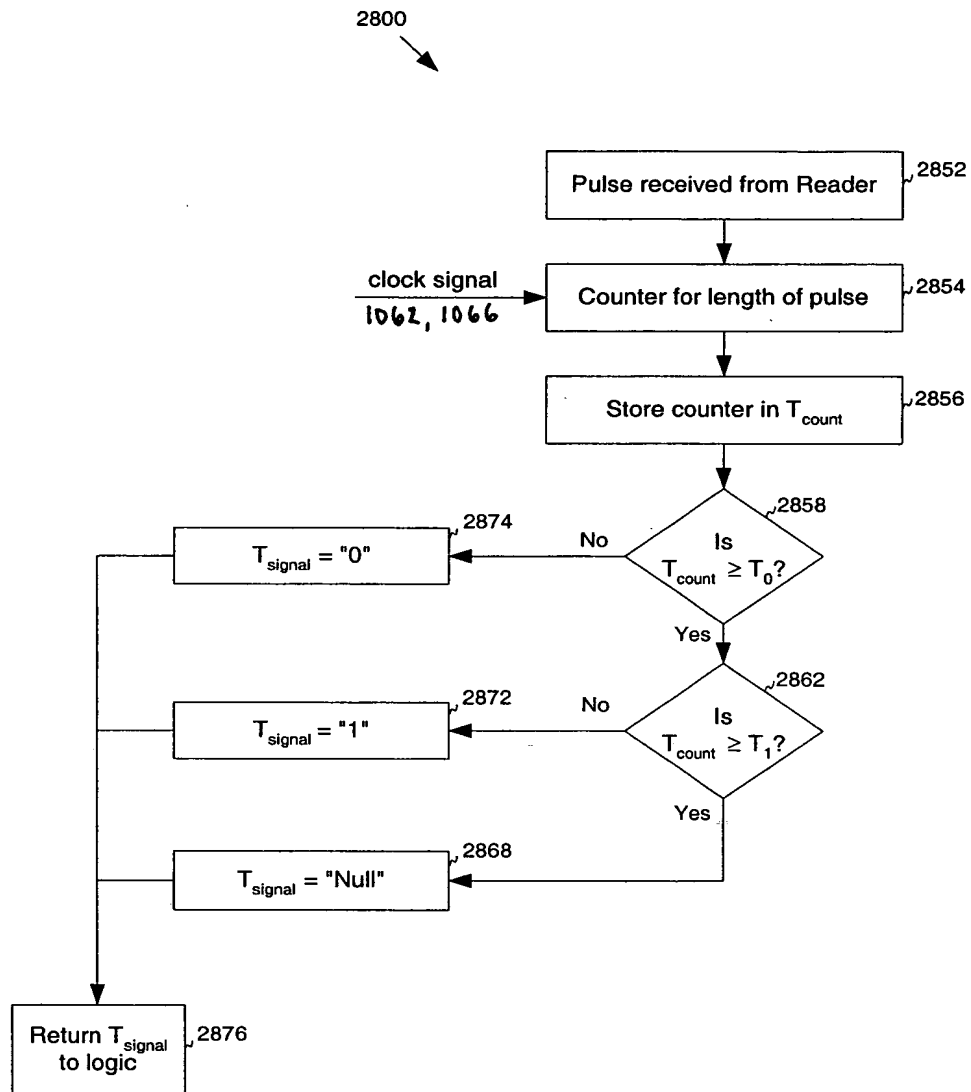
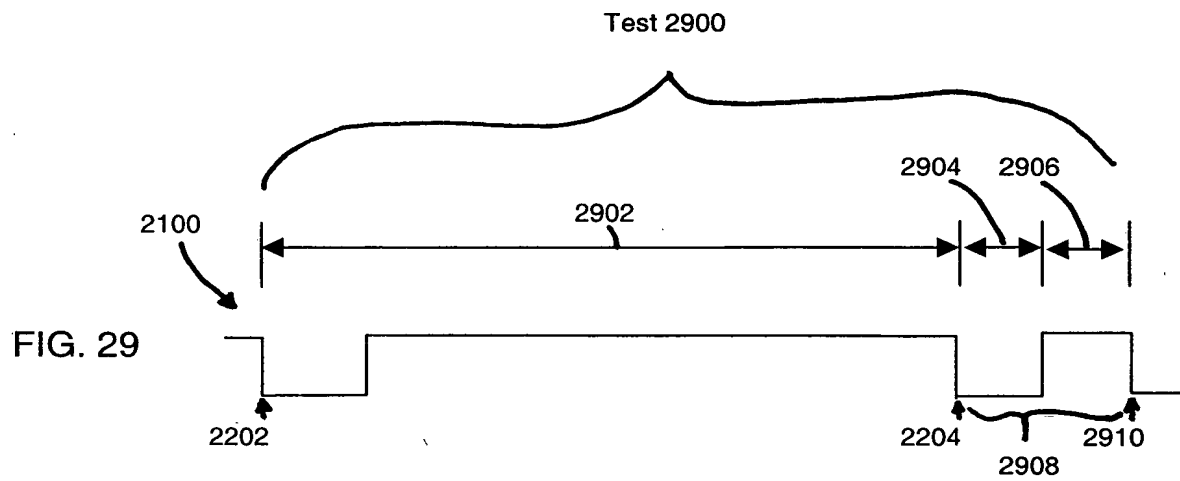


FIG. 28F



2025-09-20 10:30:00

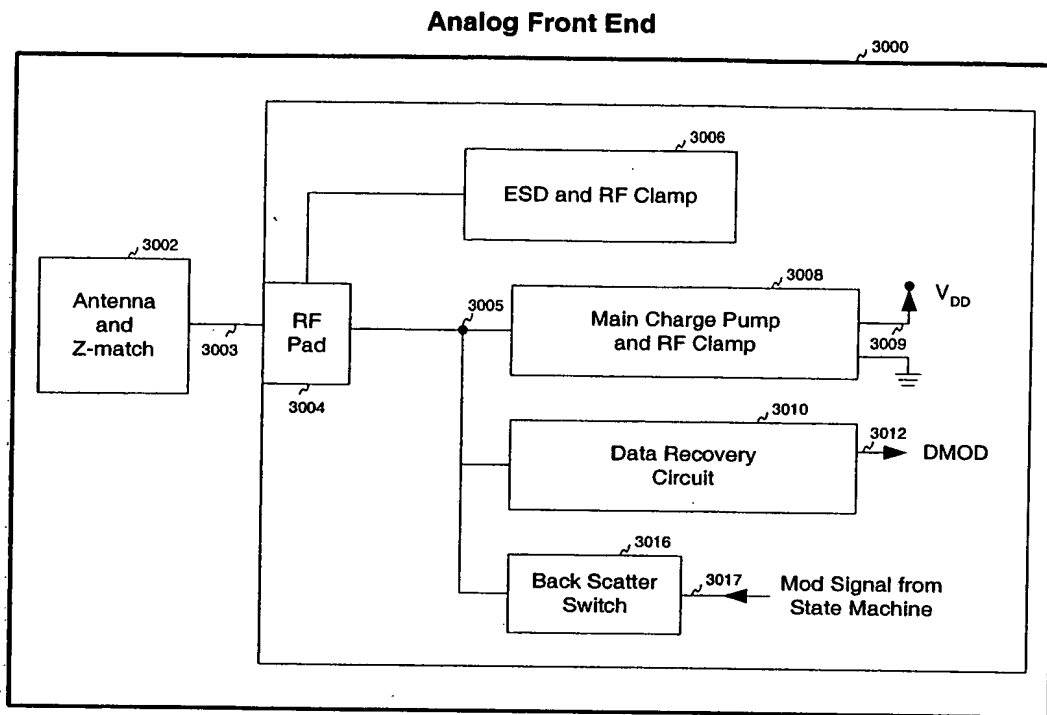


FIG. 30

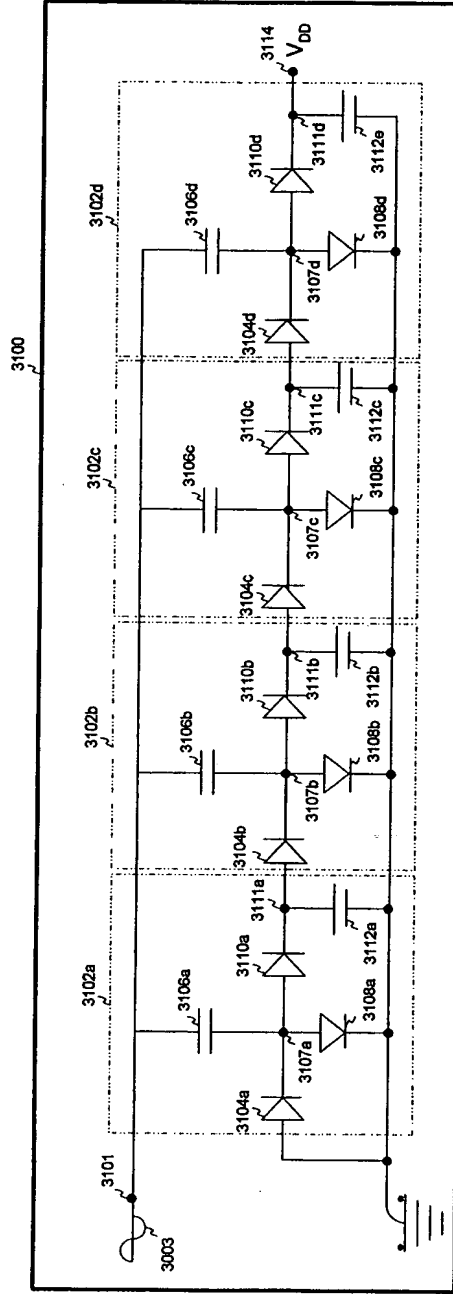


FIG. 31

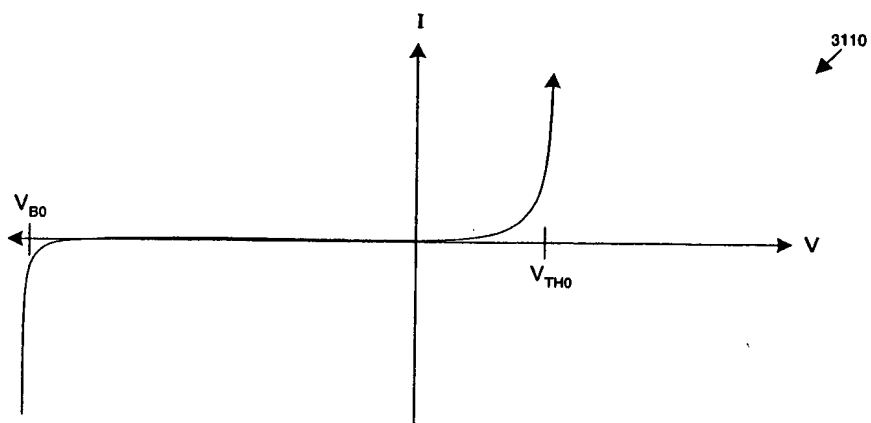


FIG. 32A

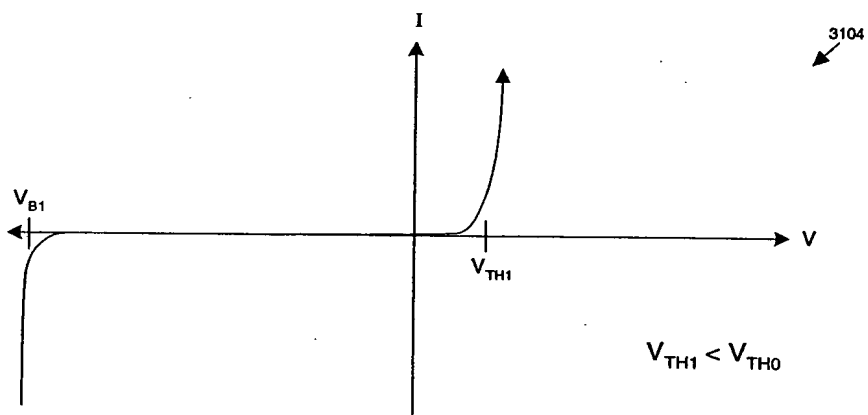


FIG. 32B

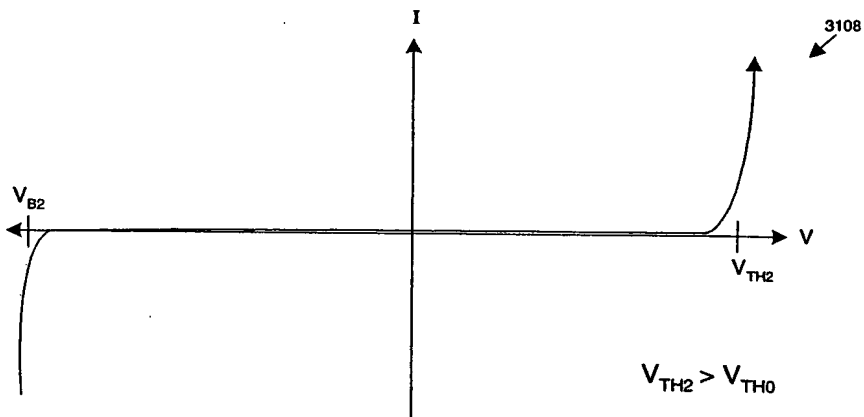


FIG. 32C

10073000-02100
2022-0002/001

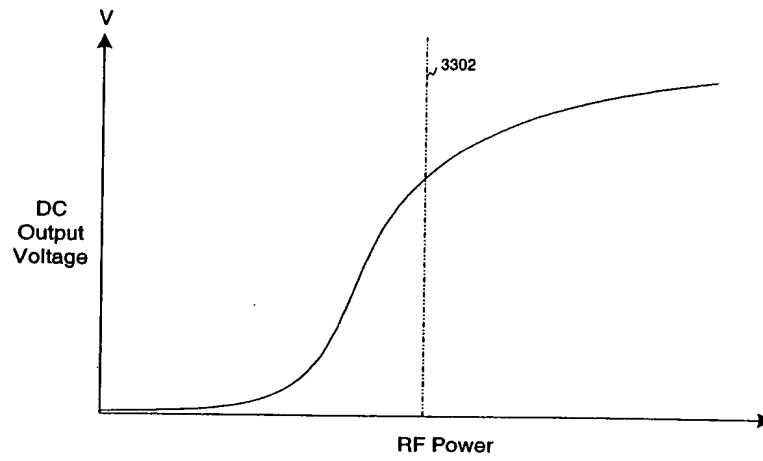


FIG. 33A

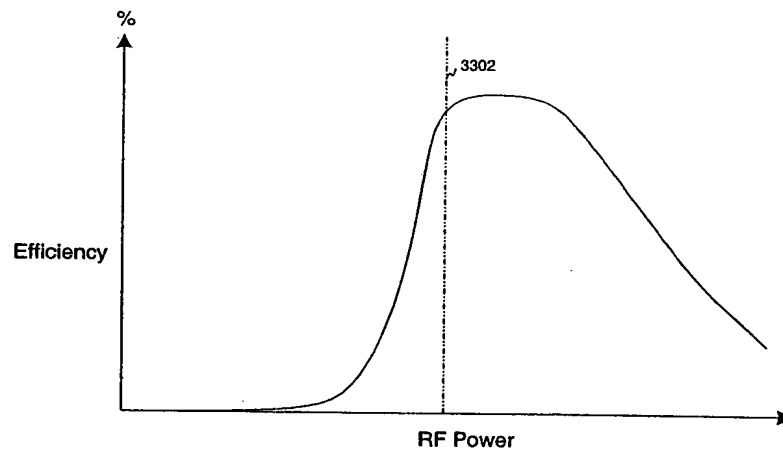


FIG 33B

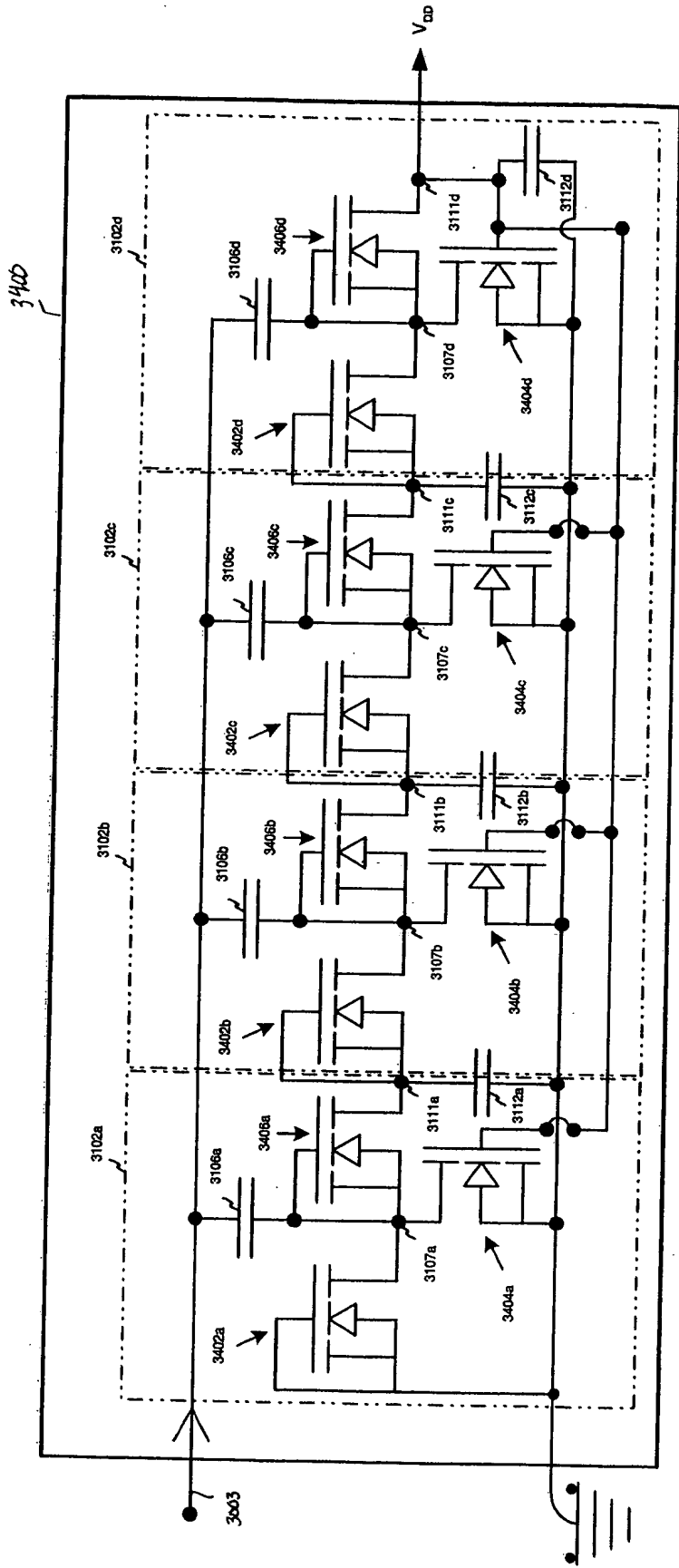


FIG. 34A

3400

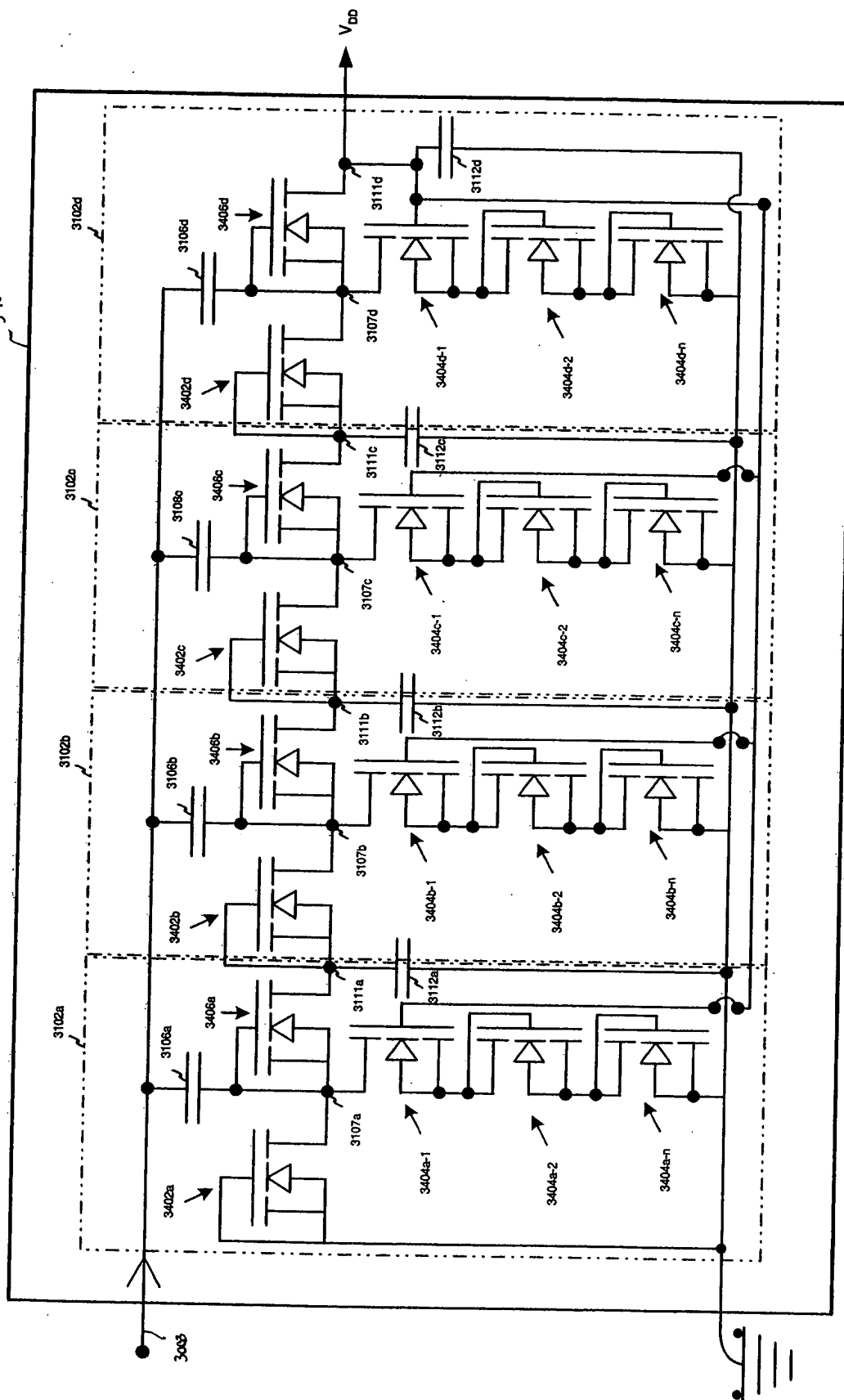


FIG. 34B

2025-08-08 10:00:00

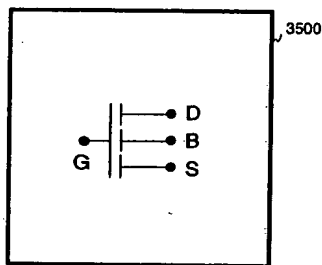


FIG. 35A

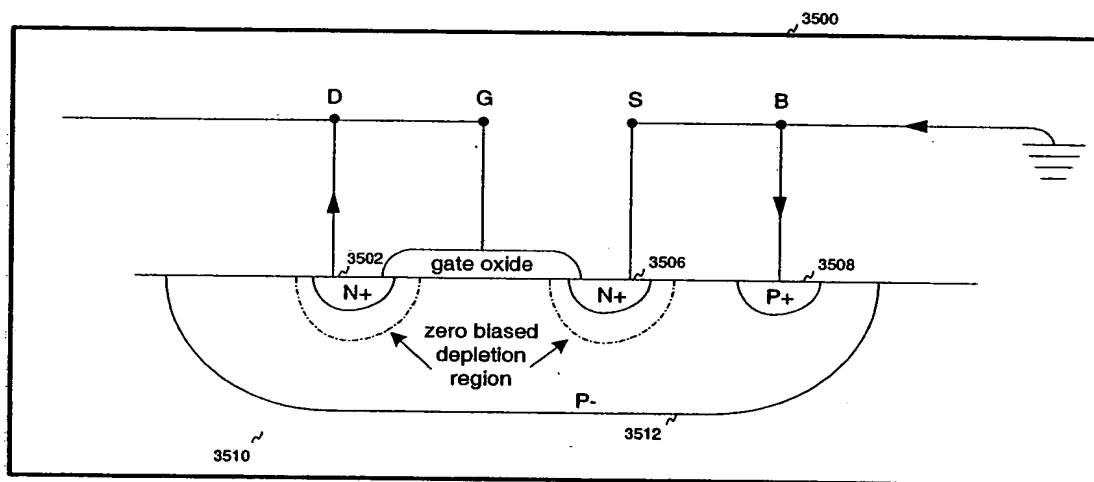


FIG. 35B

FIG. 37A

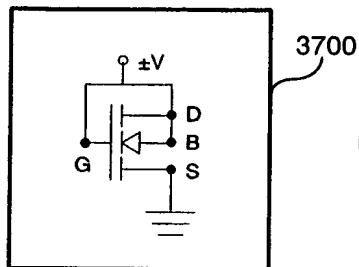


FIG. 37A

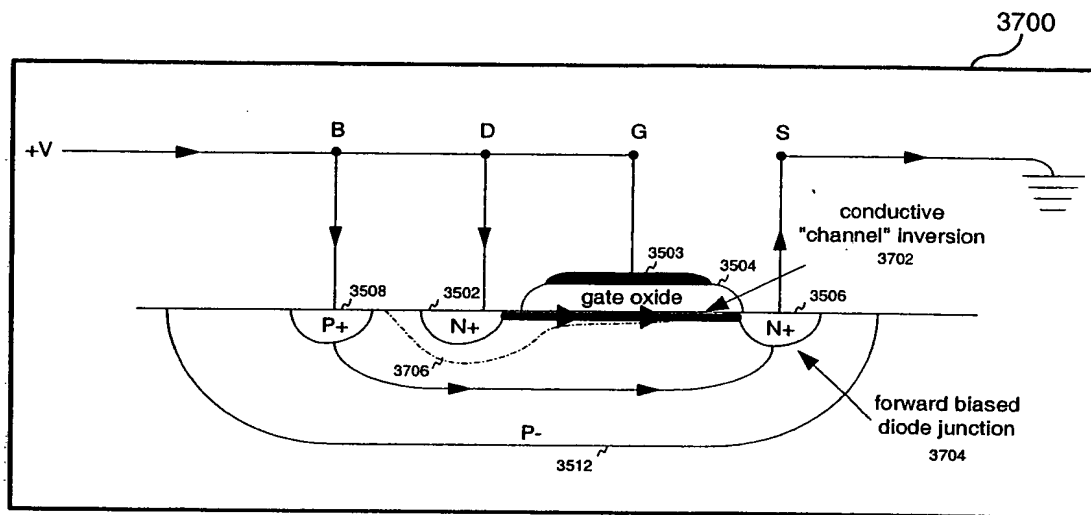


FIG. 37B

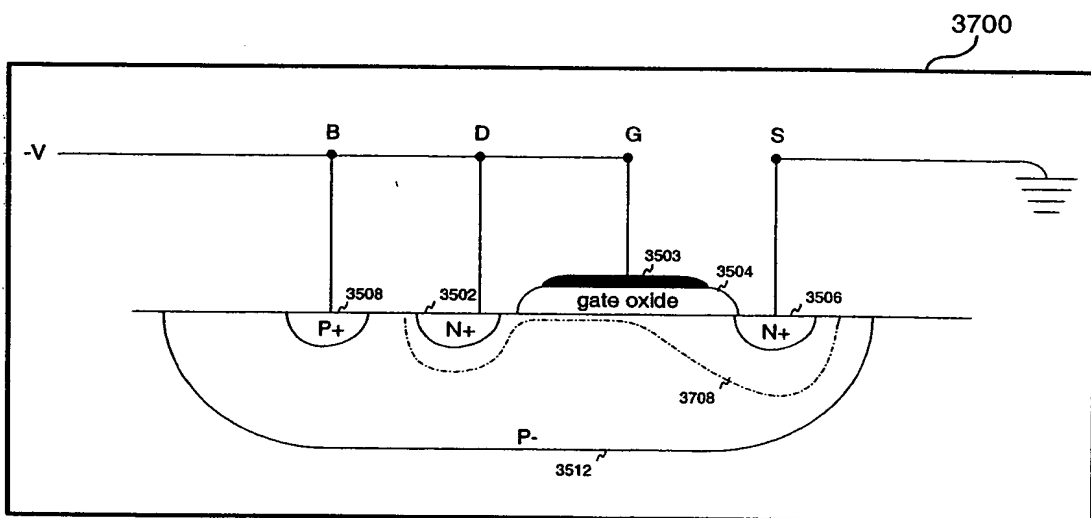


FIG. 37C

10073000-0041204

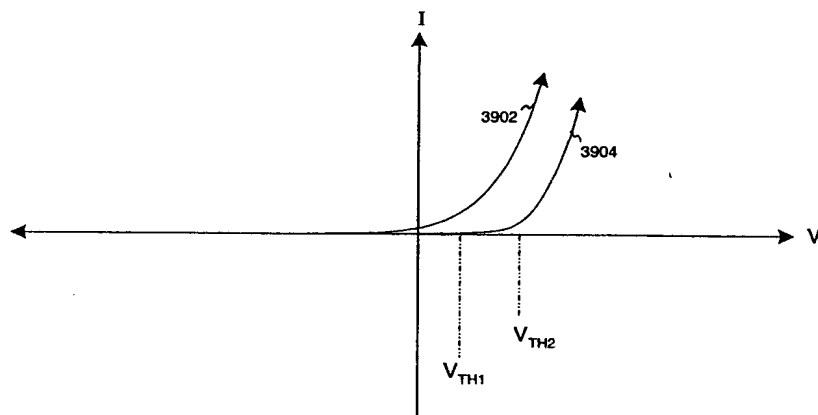


FIG. 39

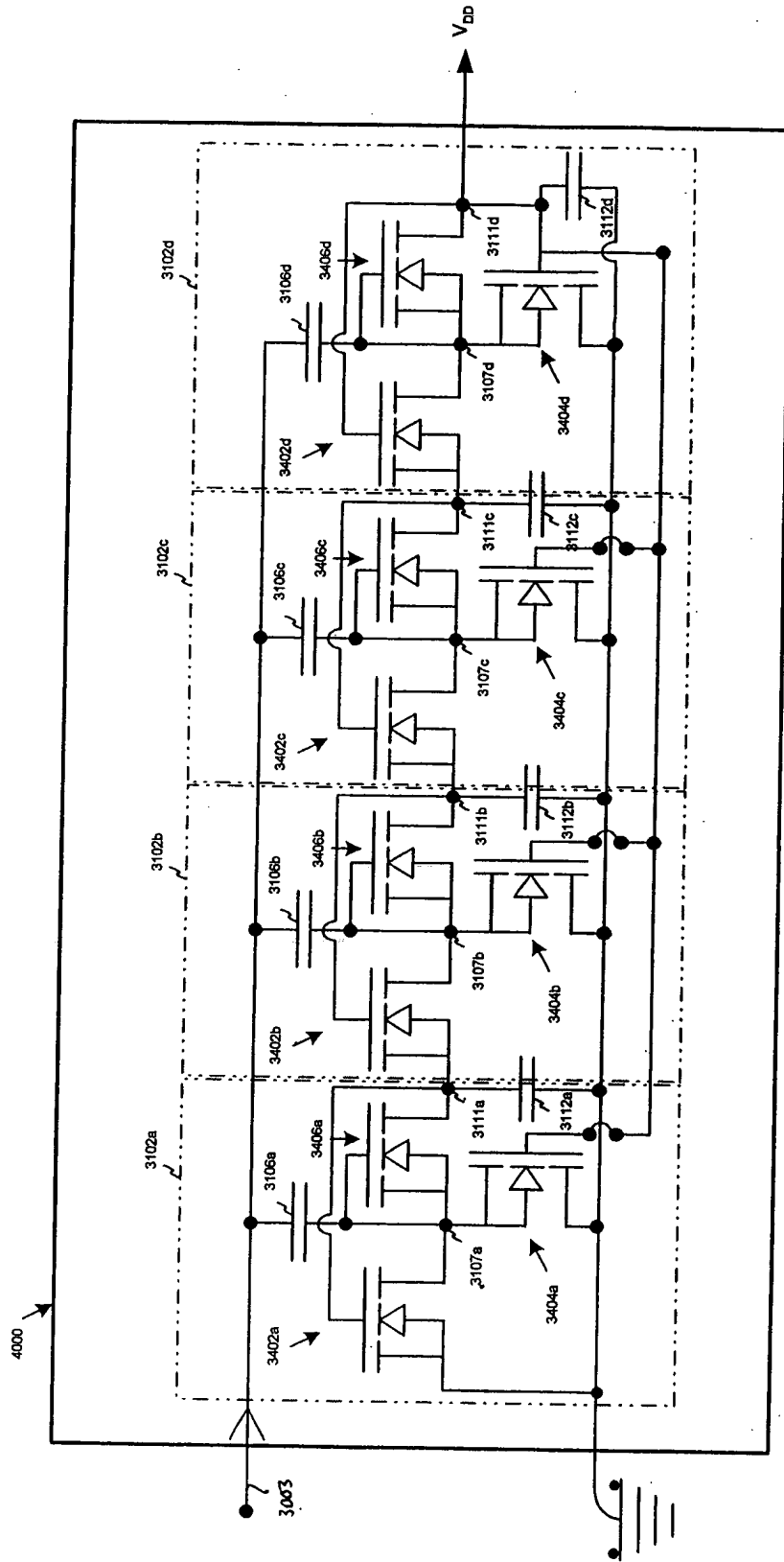


FIG. 40A

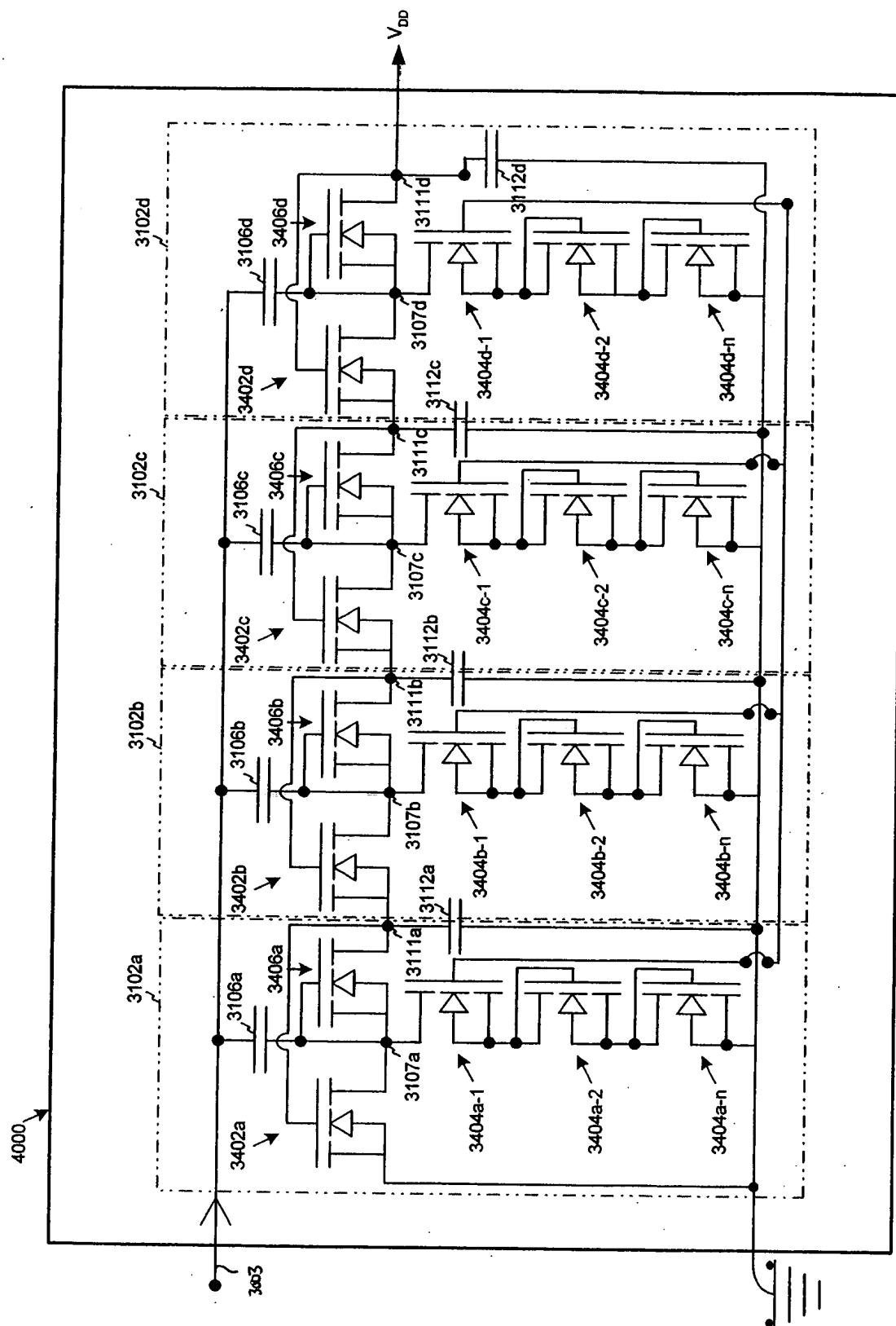


FIG. 40B

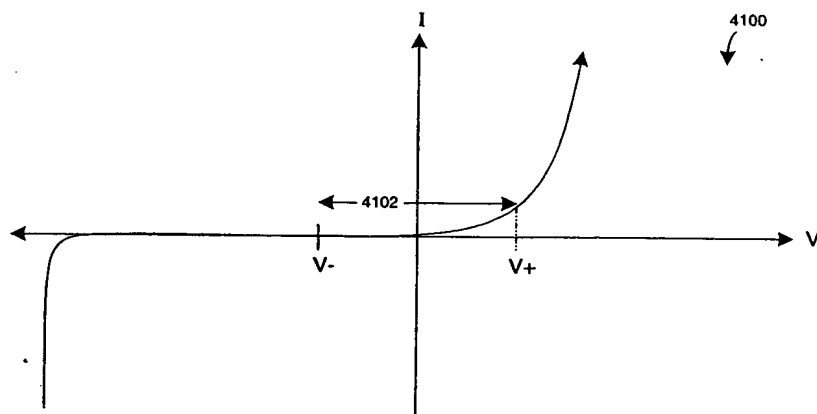


FIG. 41A

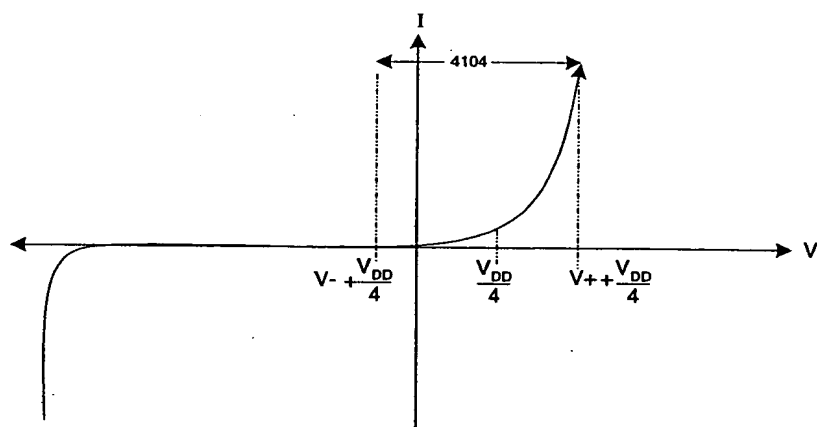


FIG. 41B

2025-03-20 09:00:00

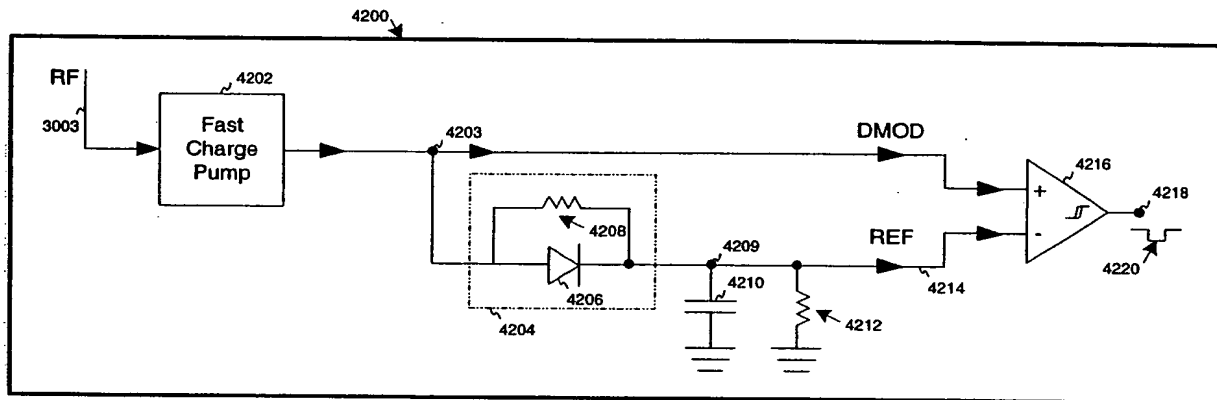


FIG. 42

2025-08-20 10:00:00

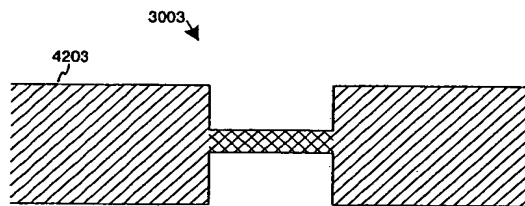


FIG. 43A

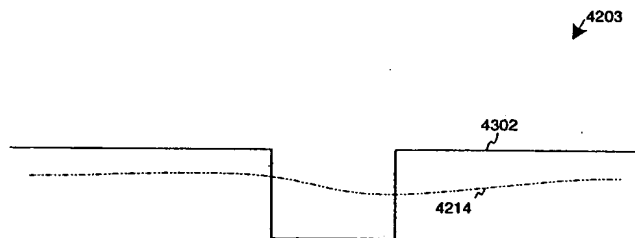


FIG. 43B

[illegible]

3

2023-08-08 10:00:00

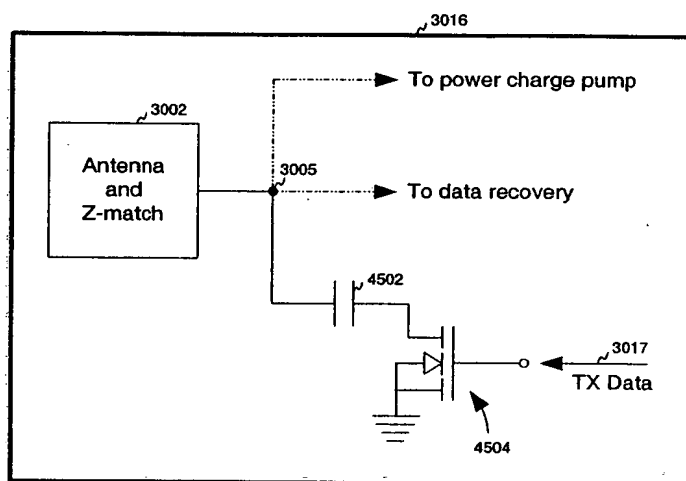


FIG. 45